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Title: SFI-4 Phase 2: 64b/66b Line Code Update

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Abstract: An update to the proposed 64b/66b line code for SFI-4 Phase 2. Uses a modified form of the 802.3ae 64b/66b code as a physical layer linecode for SFI-4 Phase 2: a protocol independent, 12.5 Gb/s, four wire, chip-to-chip interconnect interface.

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SFI-4 Phase 2: 64b/66b Line Code Update

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Topics

- Motivation
- Code Review
- Coder/Decoder Block Diagrams
- Comparison with 8B/10B
  - Eye diagram margins
  - Spectrum with static data
  - Capacitive coupling
- Summary

Motivation and Strategy

- Allow protocol-agnostic “virtual ribbon-cable” operation
- Leverage existing 64b/66b code to reduce design time and risk
- Reduce pin count, routing complexity, and power dissipation
- Eliminate deskew channel to reduce number of high-speed lines by 25%
- Minimize coding overhead to permit strong FEC

Code Overview

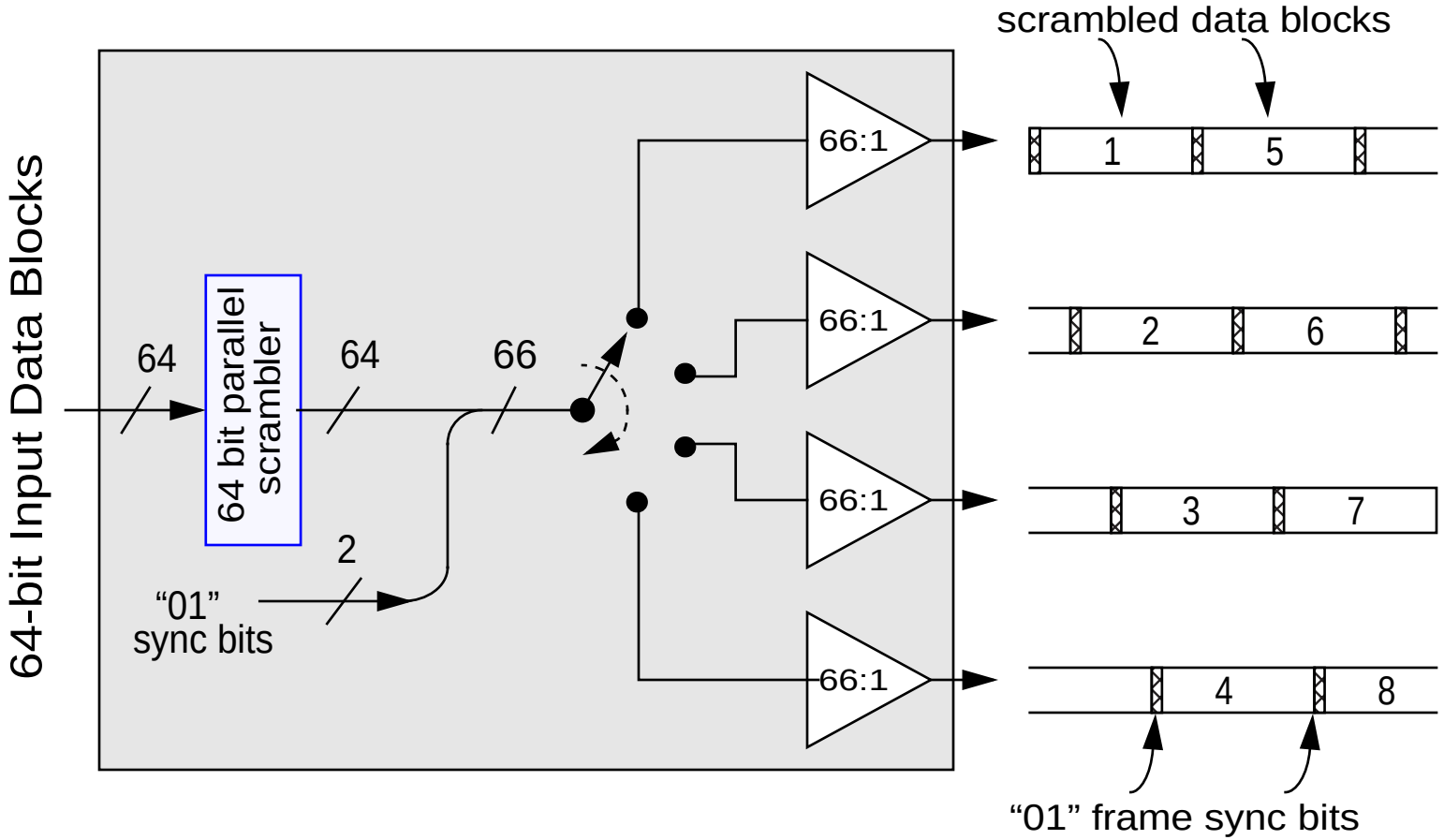
Use a simplified version of 64b/66b 10GbE linecode

- Data is transmitted in 8 byte (64-bit) blocks
- Each block is scrambled at the transmitter and descrambled at the receiver to ensure statistical DC-balance and transition density for RX PLL
- Block/byte alignment is provided by prepending each scrambled 64 bit block with two non-scrambled “01” sync bits, creating an overall 66 bit frame
- 802.3ae allows for non-data (control) frames indicated by a “10” sync pattern, but these codes are not needed, nor are proposed for SFI-4

Comparison with SONET

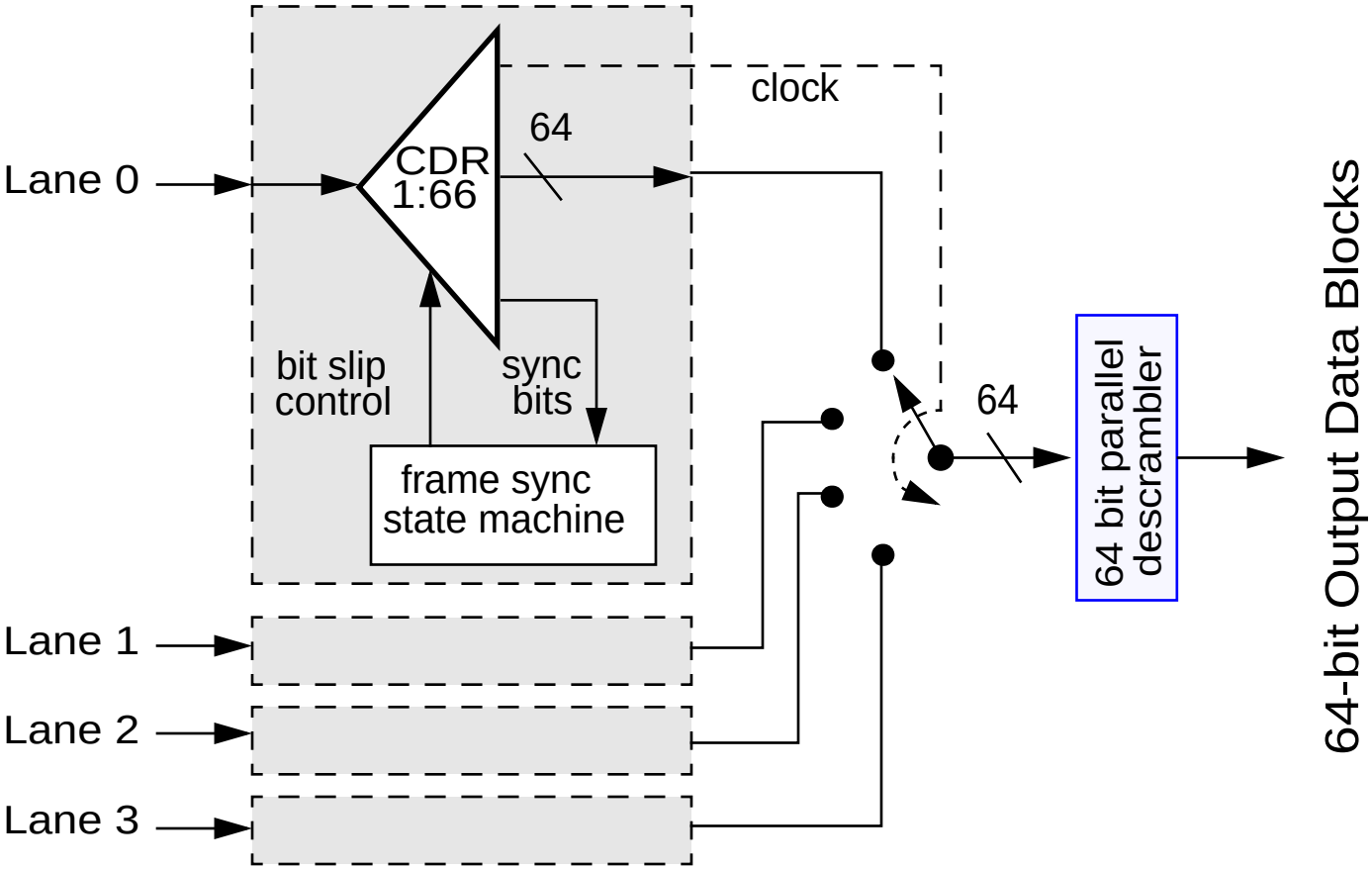
- two-bit preamble is analogous to SONET's A1/A2 sync bytes.
- SONET CDRs are designed to accommodate an 80 bit run length. This new code is deterministically limited to 64 bit run length due to the periodic preamble bits.
- Both codes use similar bit-slipping method to acquire frame sync.
- This code is similar in spirit to the SONET code. It is not in any way compatible, but inherits much of SONET properties while being much simpler to implement.
- Much less on-chip buffering required
- Lower latency

Coder Block Diagram



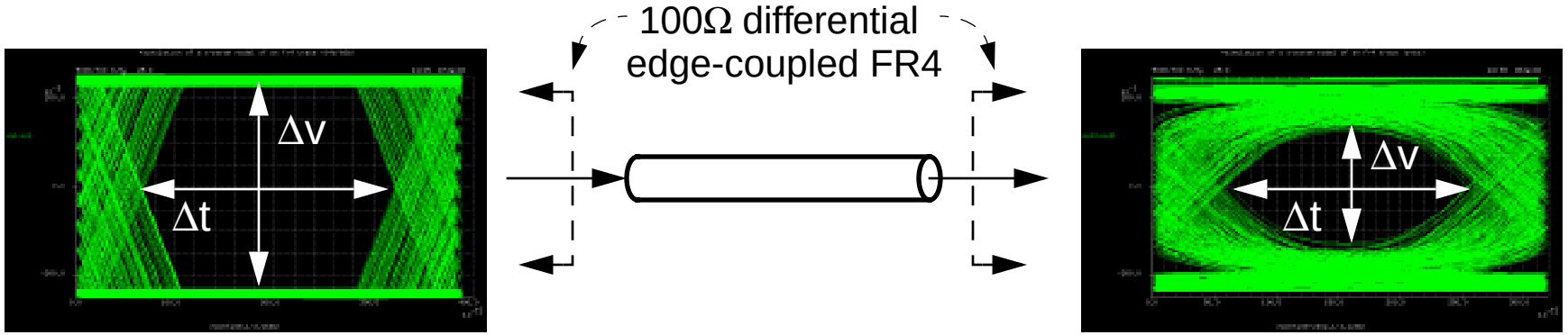
Coder is a simplified 64b/66b codec (data frames only), with 66 bit frames sent round-robin across the 4 output lanes.

Decoder Block Diagram



Deskew logic uses recovered Lane 0 clock phases to optimally sample other lanes with +/- 16 bits of skew tolerance

Eye Diagram Simulation Setup



ADS stripline model parameters:

trace spacing =10 mil, width = 5 mil, thickness = 1.17mil, tanδ = 0.03,

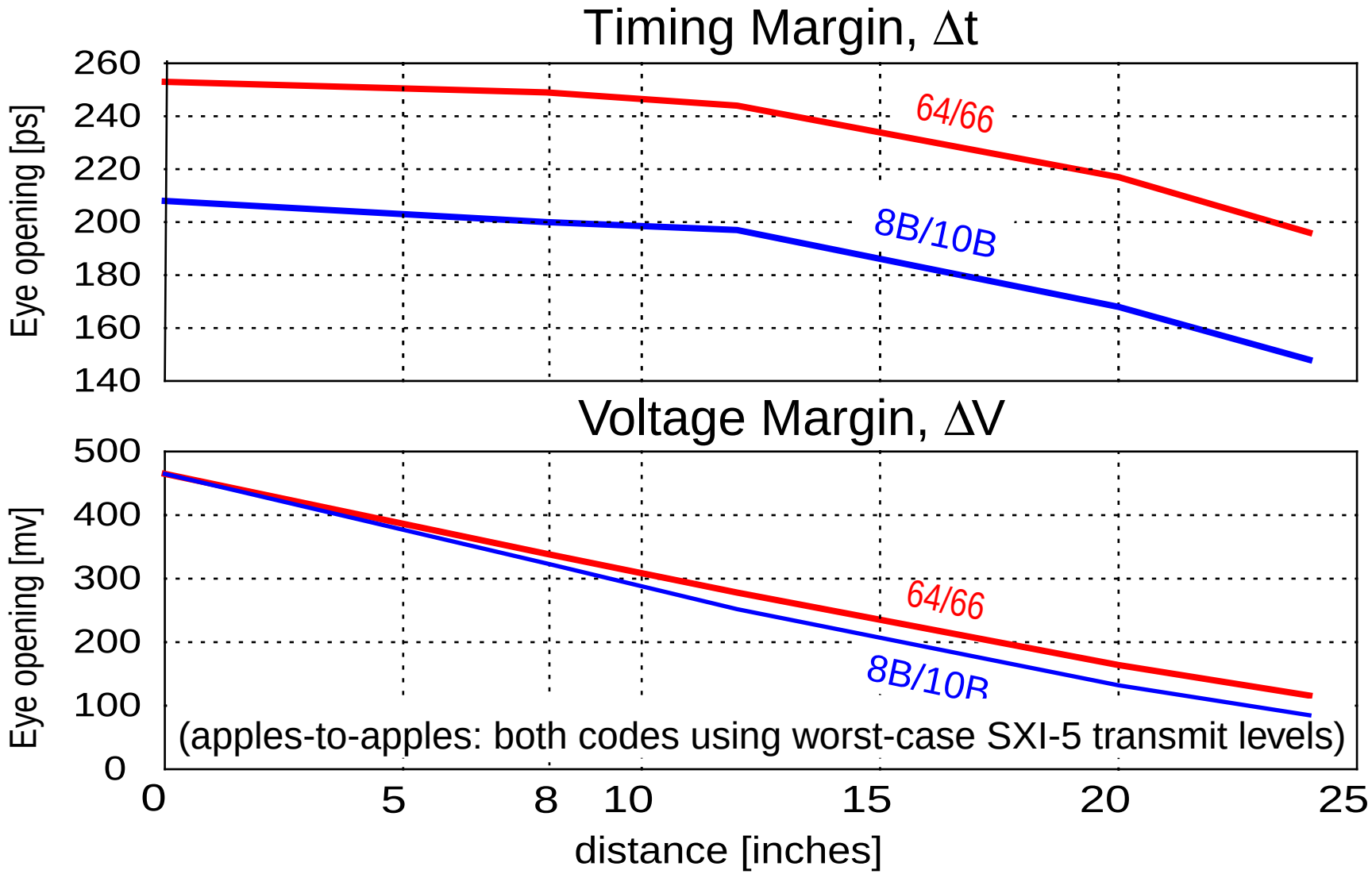
Z_0 = 50Ω, ε_r = 4.5, dielectric thickness = 16mil.

Transmitted data patterns:

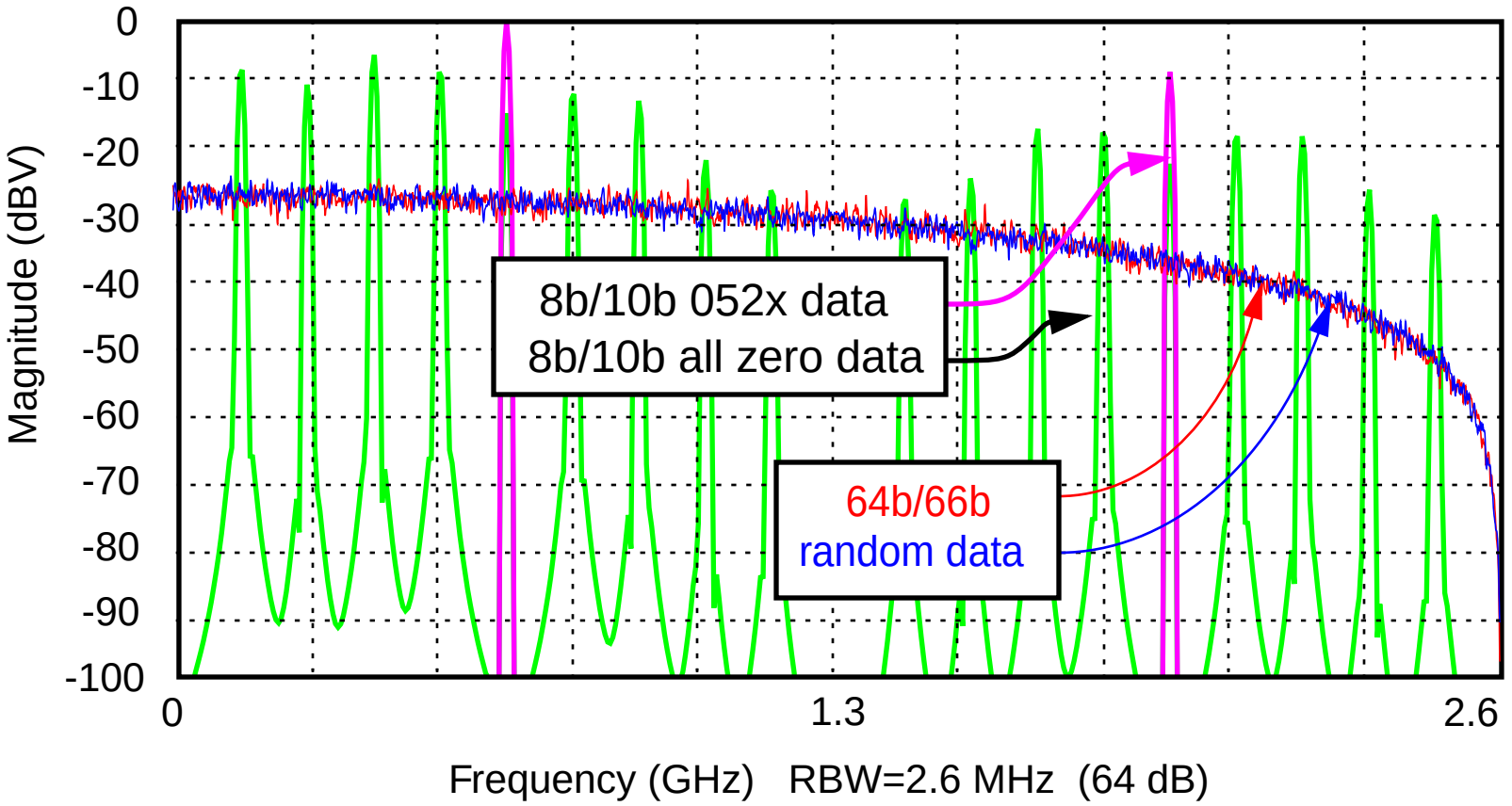
TJ=0.35UI, 463 mV pk/pk, tr/tf=83ps (worst-case SXI-5 transmit eye pattern)

- 8B/10B: x7+x6+1 pattern at 3.125 Gb/s.
- 64b/66b: 0,1 followed by 64 random bits from 2^{32}-1 pattern at 2.58Gb/s.

8b/10b, 64b/66b Simulated Eye Margins

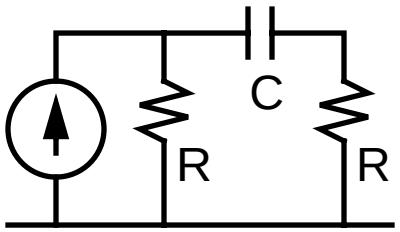


Spectral Properties



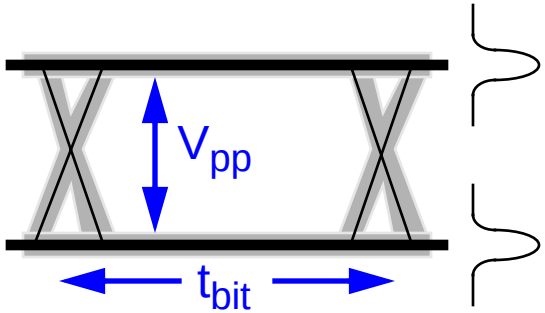
8b/10b spectrum is not well behaved with static input data patterns. 64b/66b is data agnostic.

Baseline Wander



A typical laser system will require a coupling capacitor at both TX and RX

time constant (tau) = 2*R*C



Eye diagram shows Gaussian wander (with stddev of sigma) due to statistical of 1's and 0's in charging coupling capacitor C.

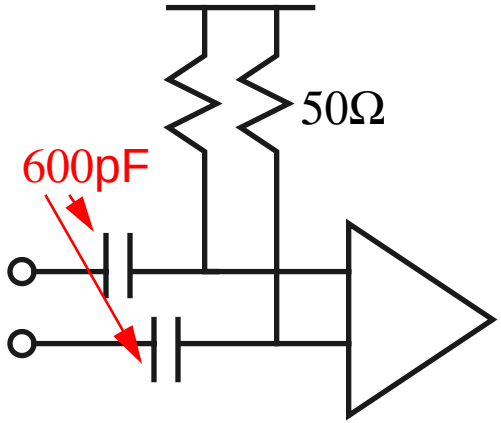
The average value of N random bits is 1/2 with a sigma of 1/sqrt(N)
A coupling capacitor can be approximately considered to be performing a moving average over N bits, where N ~= 8*tau/(tbit)

$$\sigma(offset) = V_{pp}\sqrt{\frac{t_{bit}}{8\tau}}$$

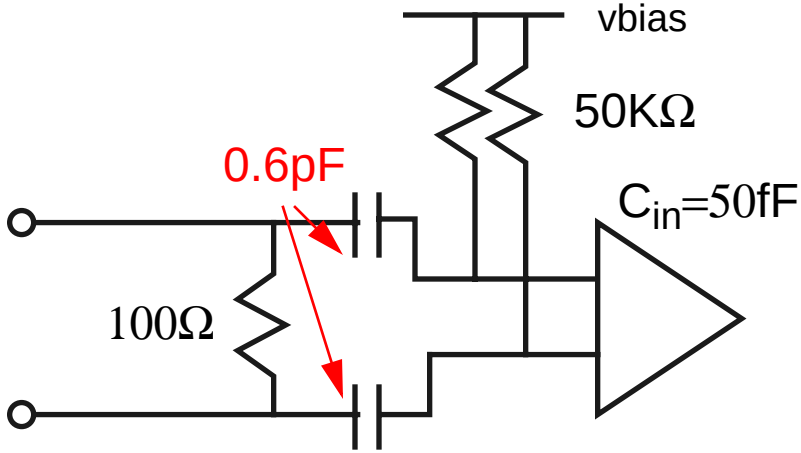
coupling capacitor analysis

$$\sigma(offset) = V_{pp}\sqrt{\frac{t_{bit}}{8\tau}}$$

tbit = 388pS, Vpp=500mV, if we desire <100mV total baseline wander at 10^{-12} BER, then σ=20mV, therefore τ = 30nS. At 50Ω impedance we need 600pF, at 50KΩ impedance, we only require 0.6pF!



old style input stage



input stage optimized for on-chip capacitors

Summary

- Eliminates deskew lanes
- Fits within 70 pin connector
- Ensures DC balance on all lanes
- Limits run-length to a maximum of 66 bits
- Single 64b/66b codec required
- Simple deskew accomodates 16 bits of skew
- 3.125% coding overhead
- Protocol Agnostic (virtual ribbon cable)
- Leverages existing 802.3ae 64b/66b code