Clock and Data Recovery for Serial Digital Communication

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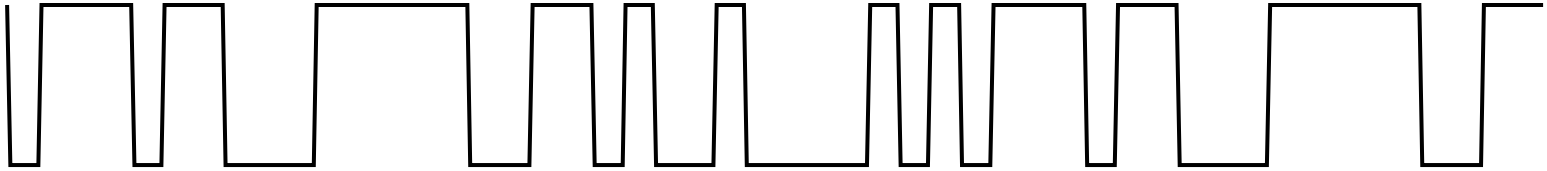
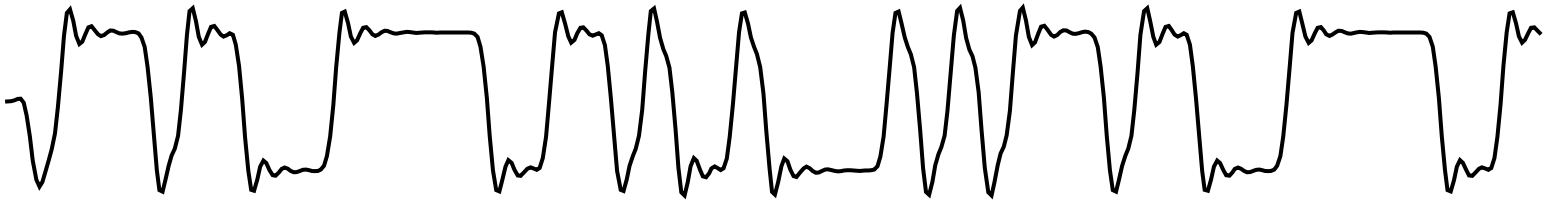
Basic Idea

Serial data transmission sends binary bits of information as a series of optical or electrical pulses:

`01110110001111100110100100001010111011000111111..`



The transmission channel (coax, radio, fiber) generally distorts the signal in various ways:

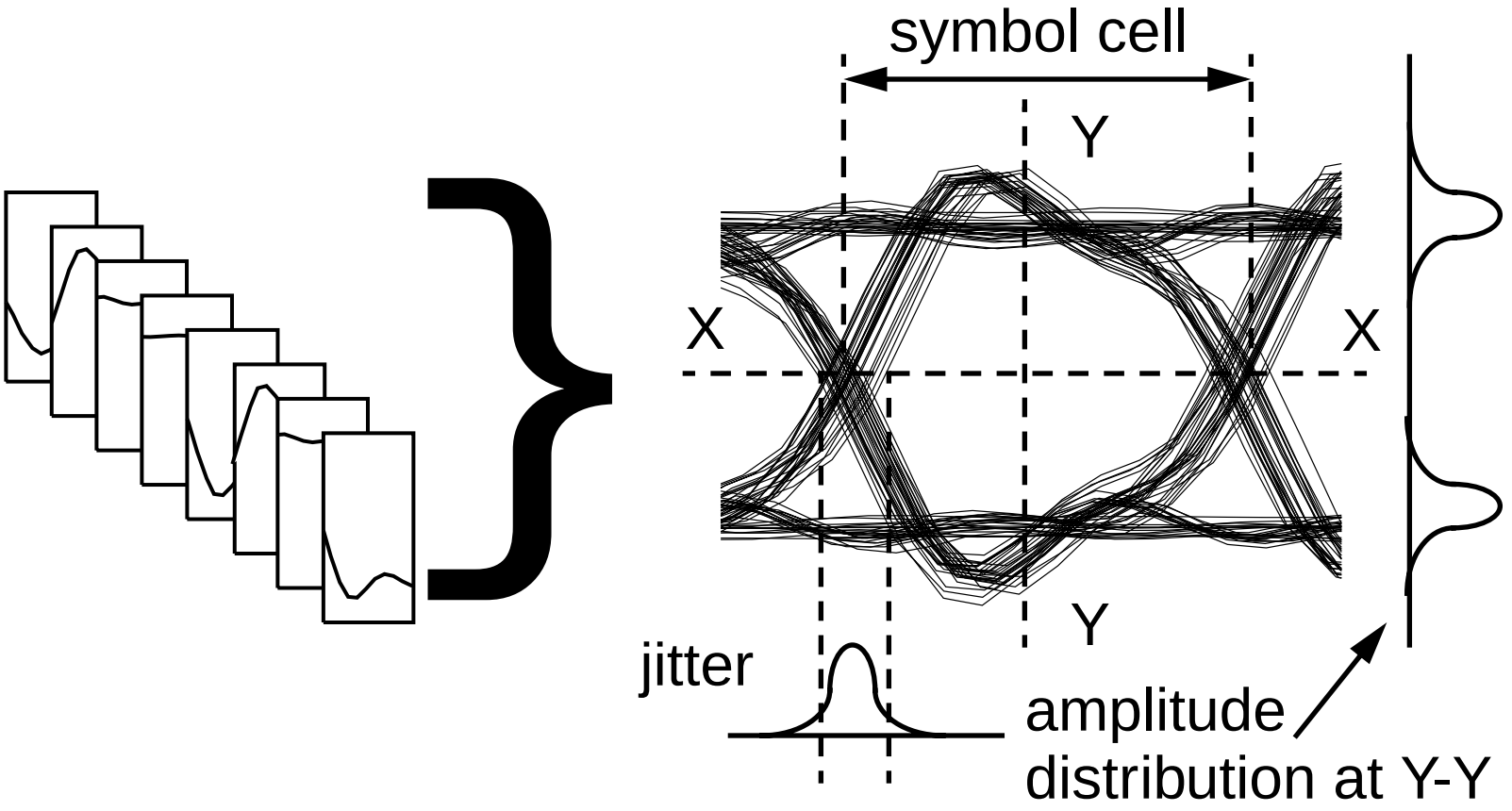


From this signal we must recover both clock and data

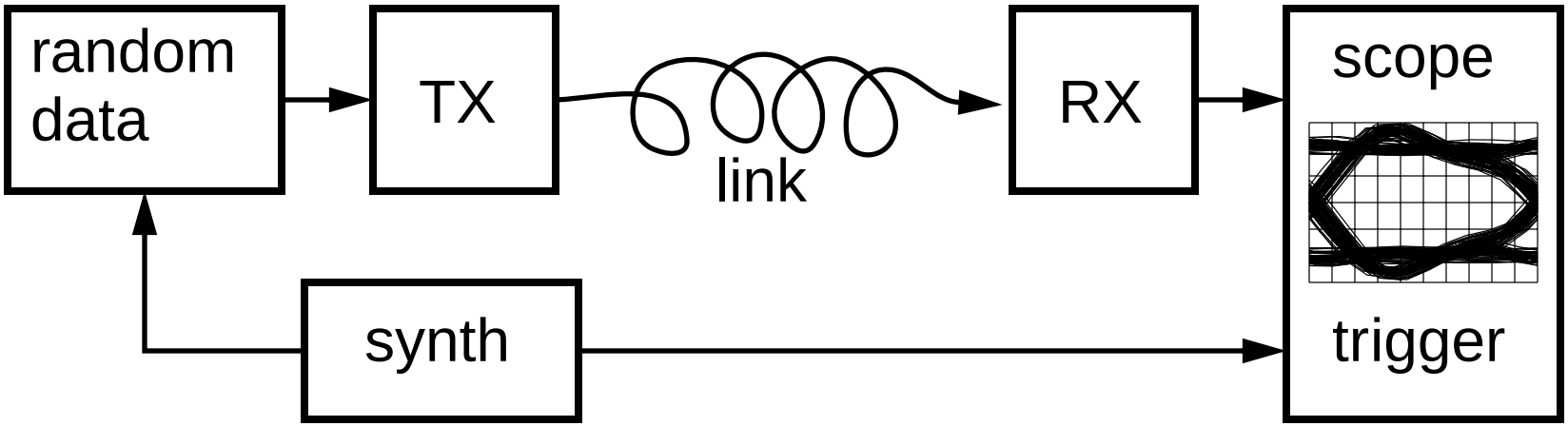
Eye diagram

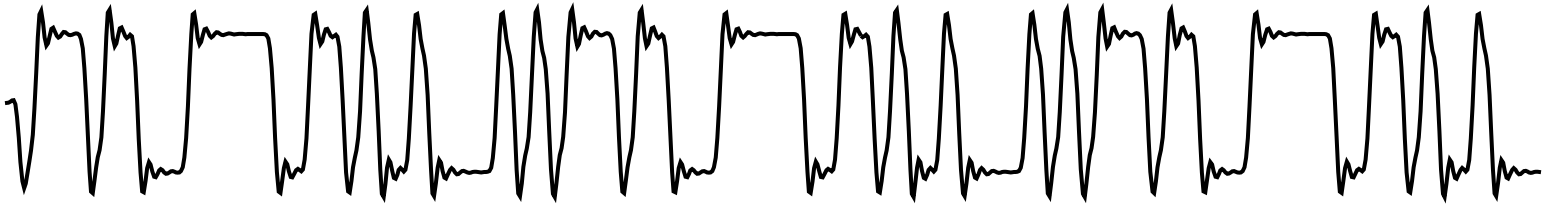
Use a precise clock to chop the received data into periods

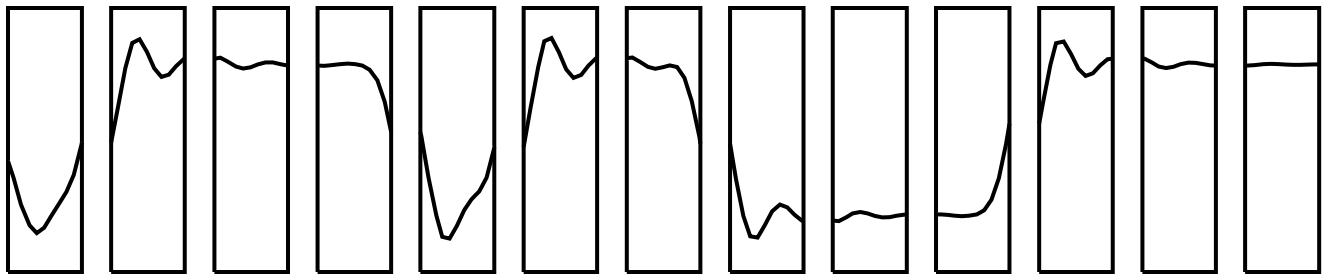
Overlay each of the periods onto one plot



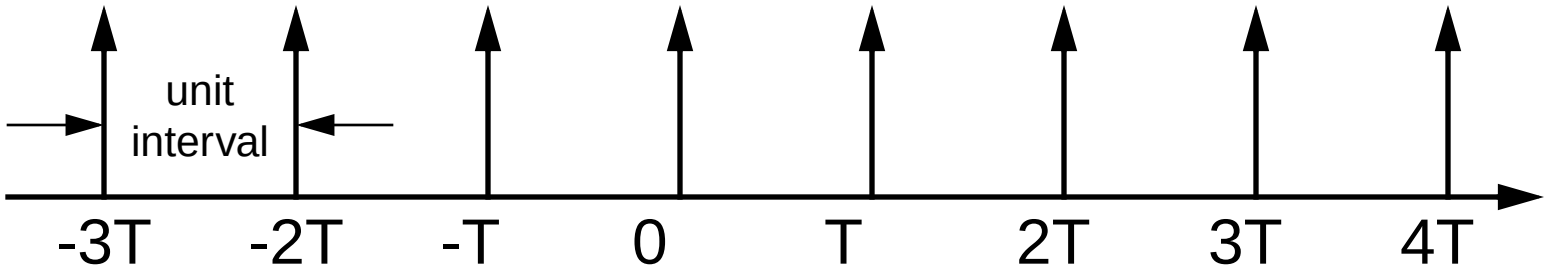
Eye diagram construction



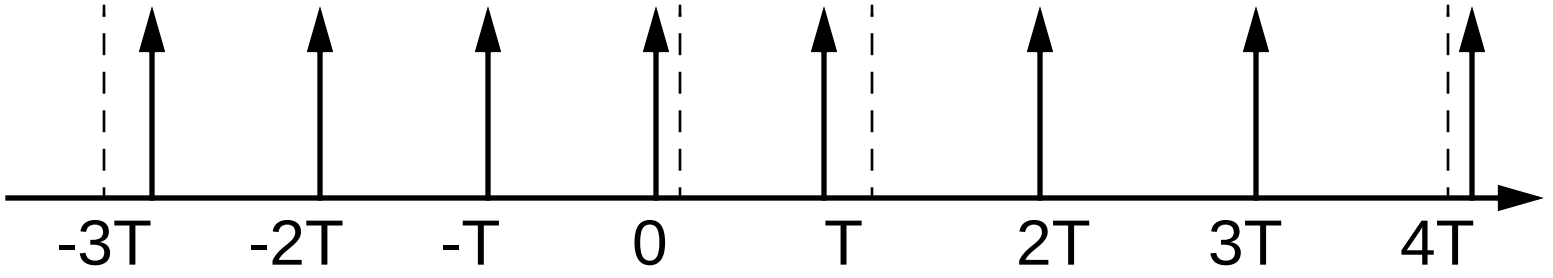




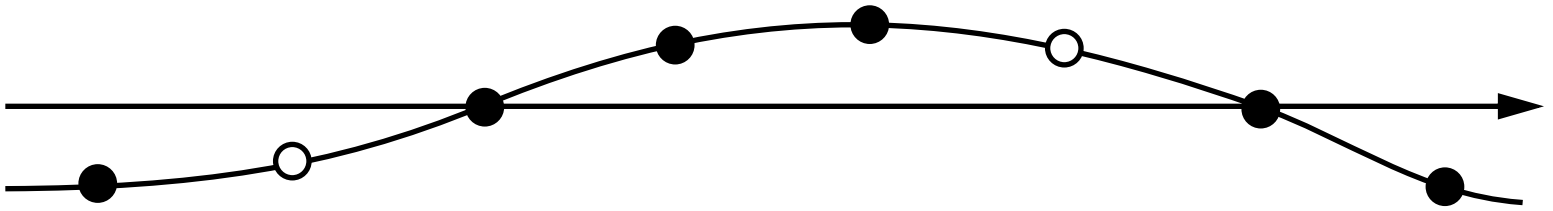
Definition of Jitter



Impulses spaced equally in time (jitter free signal)



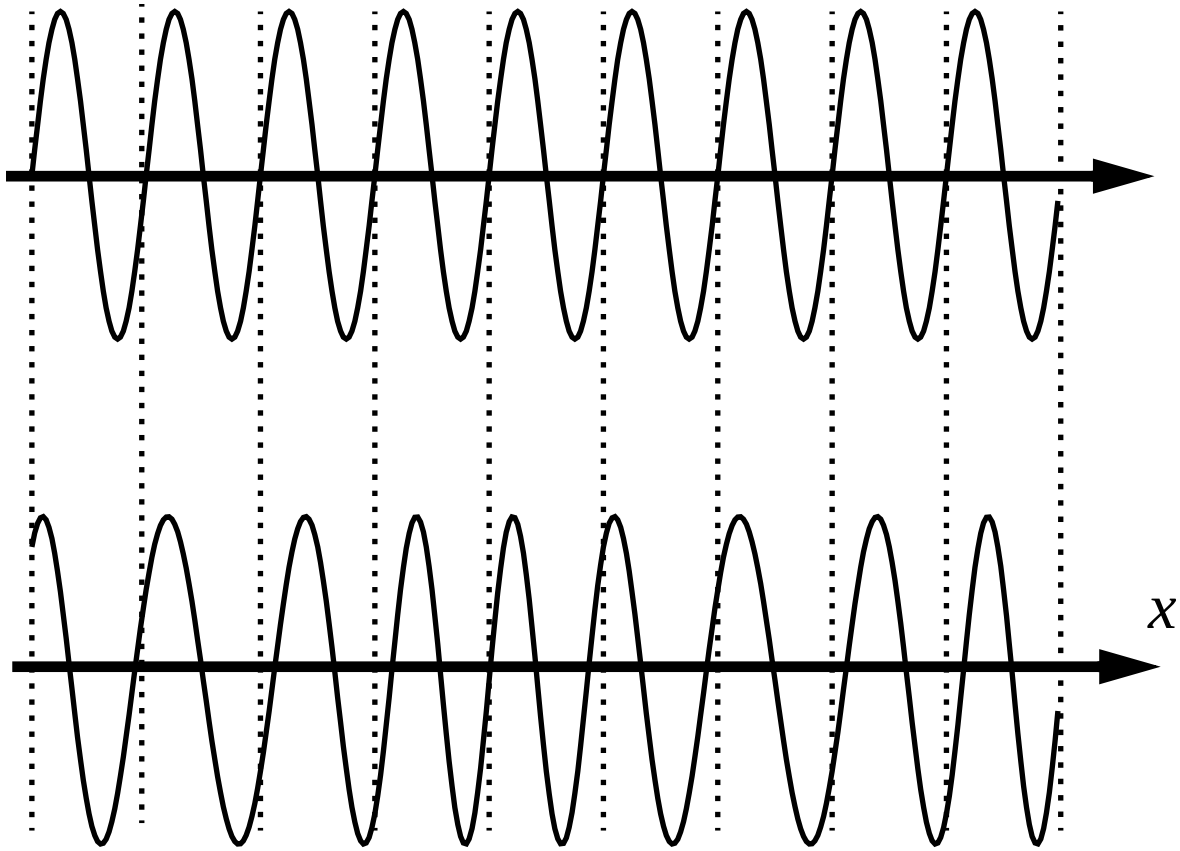
Impulses spaced irregularly in time (jittered signal)



Errors treated as discrete samples of continuous time jitter

After Trischitta and Varma: “Jitter in Digital Transmission Systems”

Analytic Treatment of Jitter



Perfect Clock:

$$x(t) = A\cos\omega_c t$$

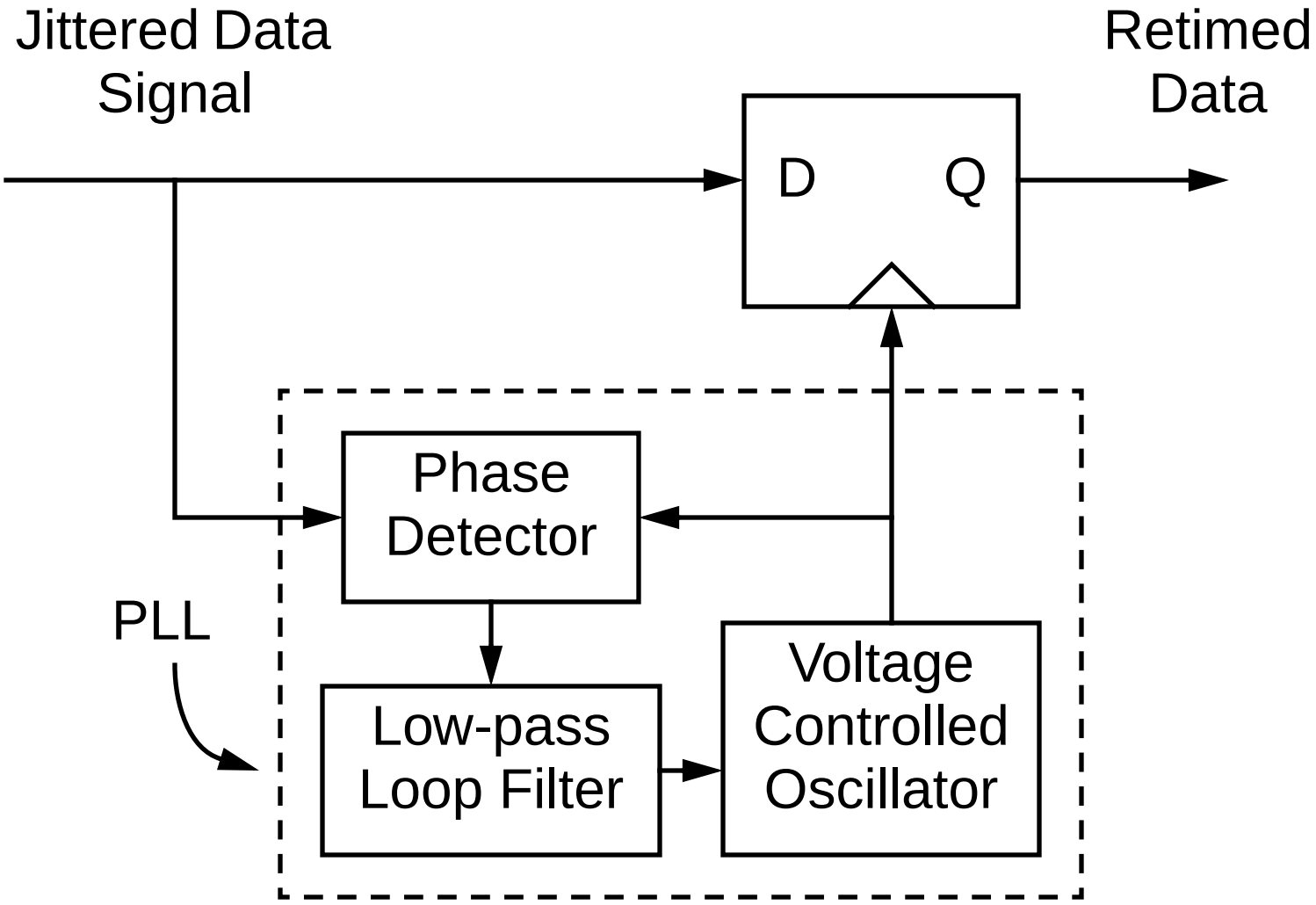
Jittered Clock:

$$x(t) = A\cos[\omega_c t + \phi(t)]$$

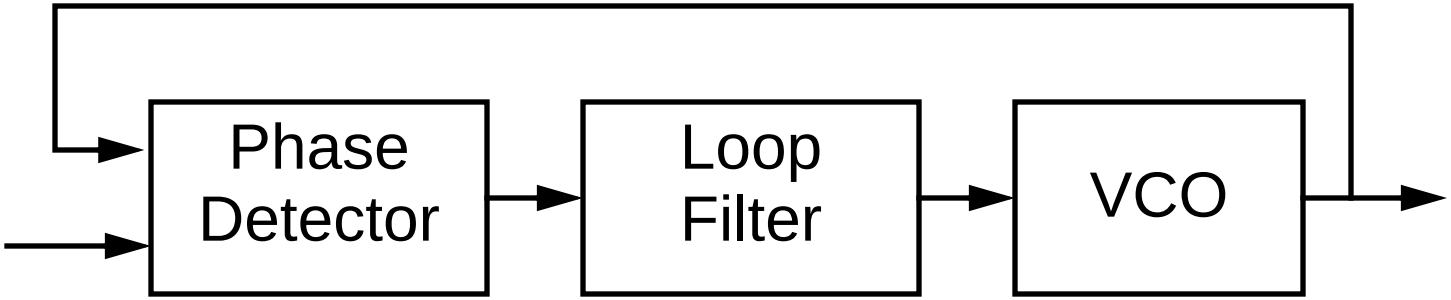
$\phi(t)$ is then treated as a continuous time signal

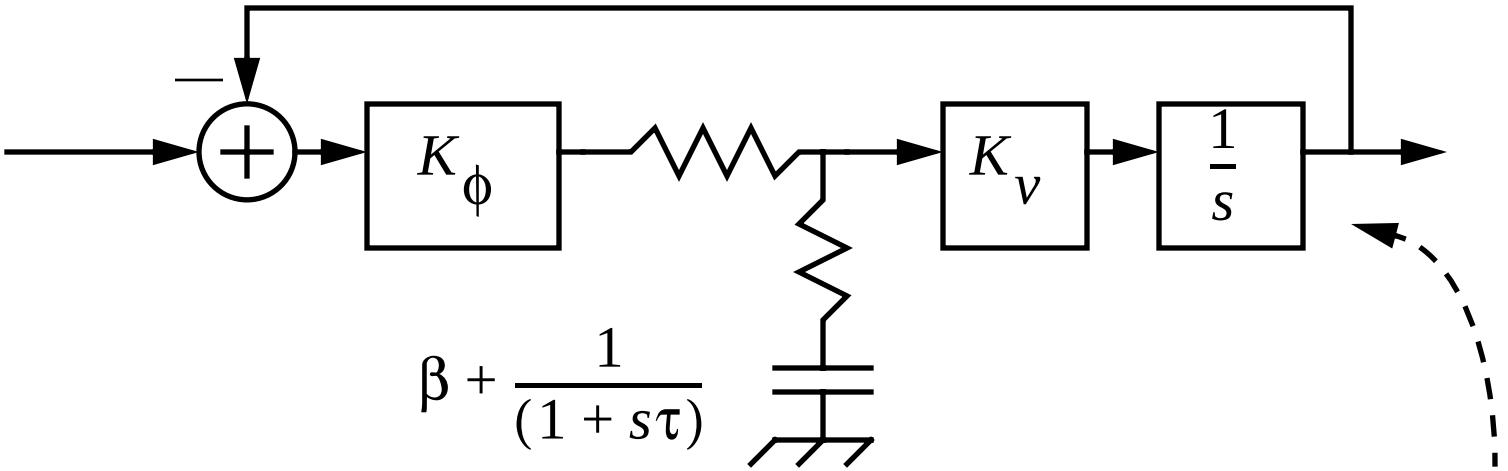
After Behzad Razavi: “Monolithic Phase-Locked Loops, ISSCC96 Tutorial”

Data Recovery with simple PLL



Model of Loop

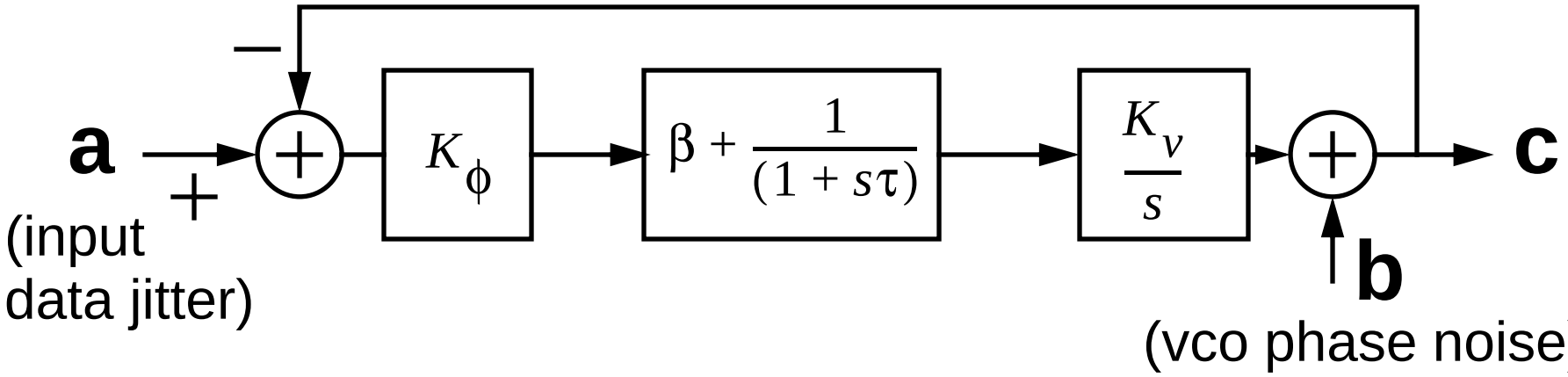


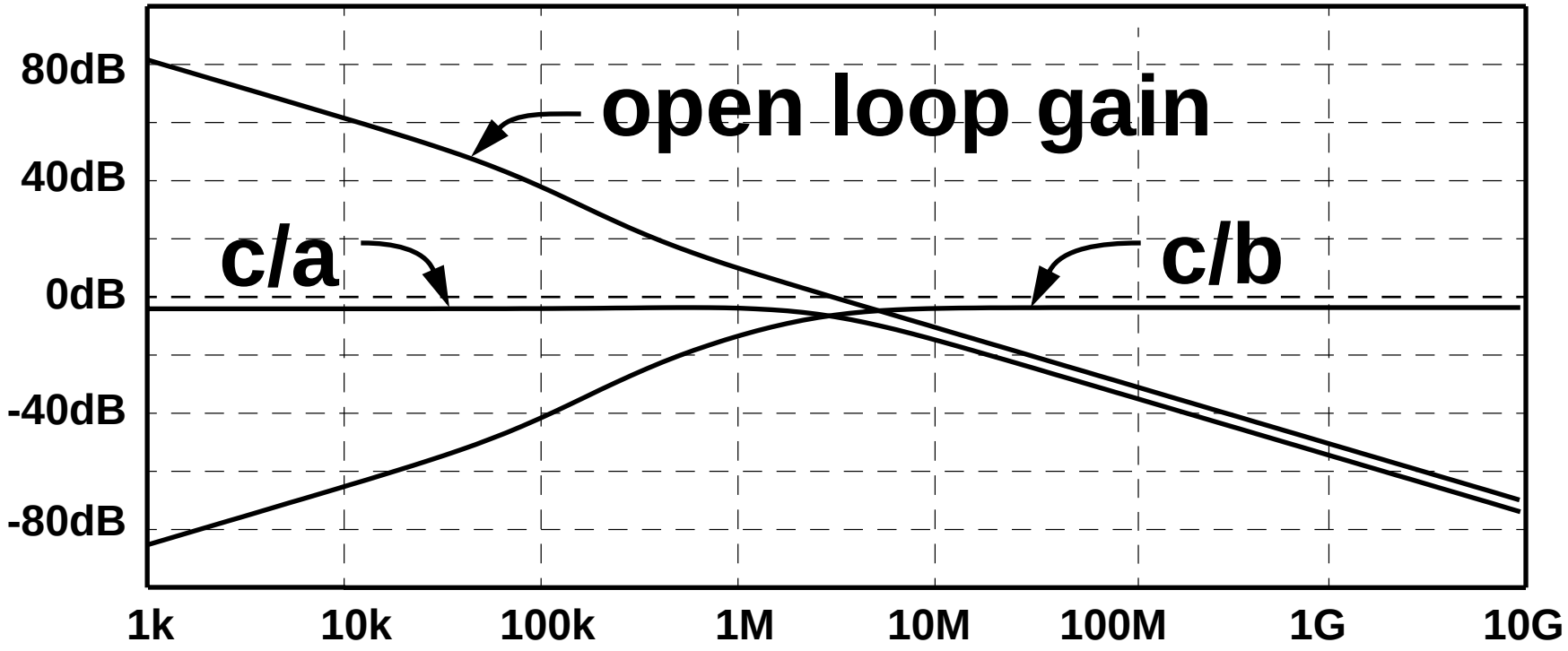


Warning: Extra Integration in loop makes for tricky design!

See Floyd M. Gardner, “Phaselock Techniques”, John Wiley and Sons, for good introduction to PLL theory

Loop Frequency Response



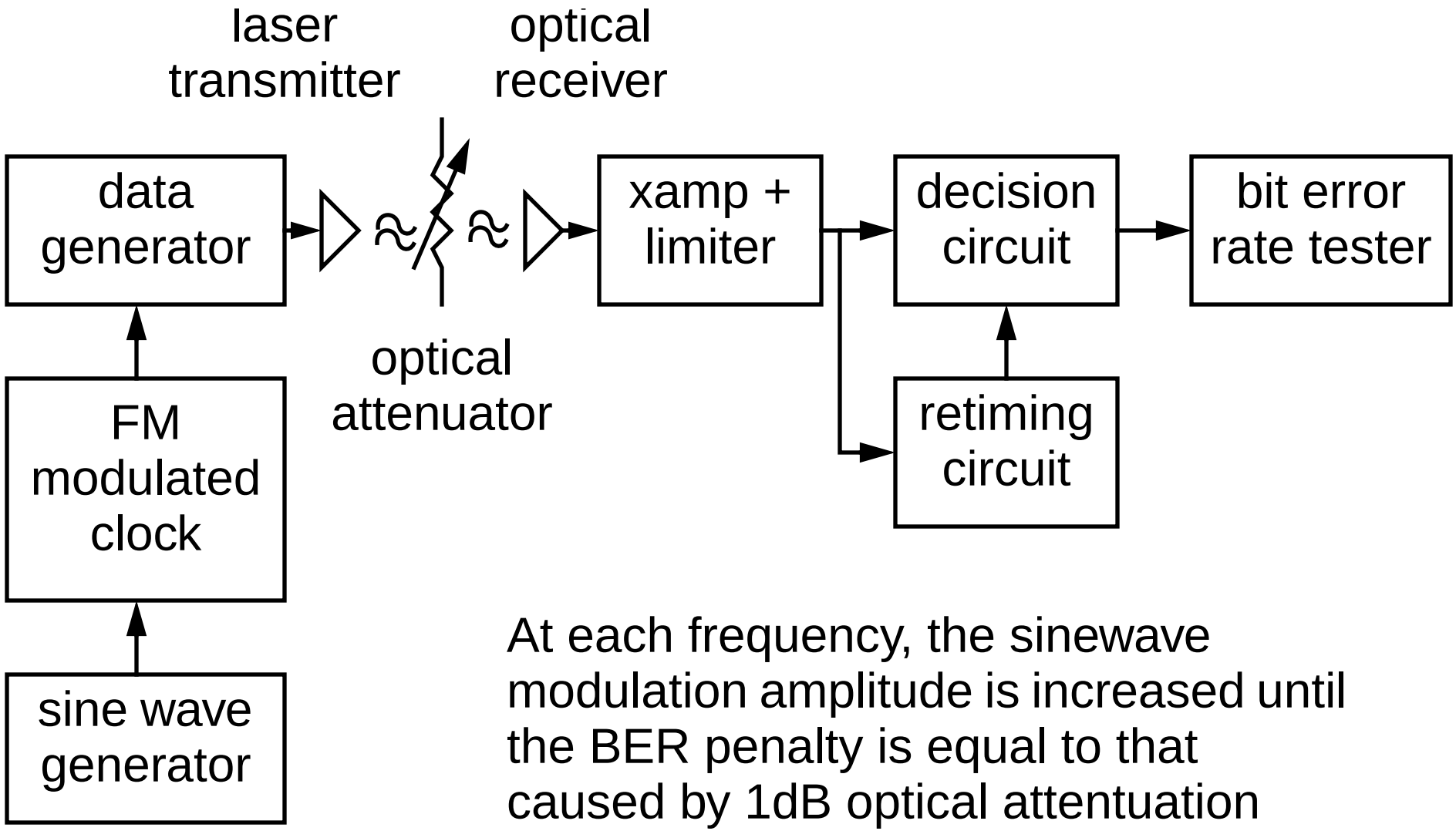


Jitter Measurements

- SONET has most complete set of jitter measurement standards, but the techniques are useful and relevant for datacom applications also.

  - Jitter Tolerance
  - Jitter Transfer
  - Jitter Generation

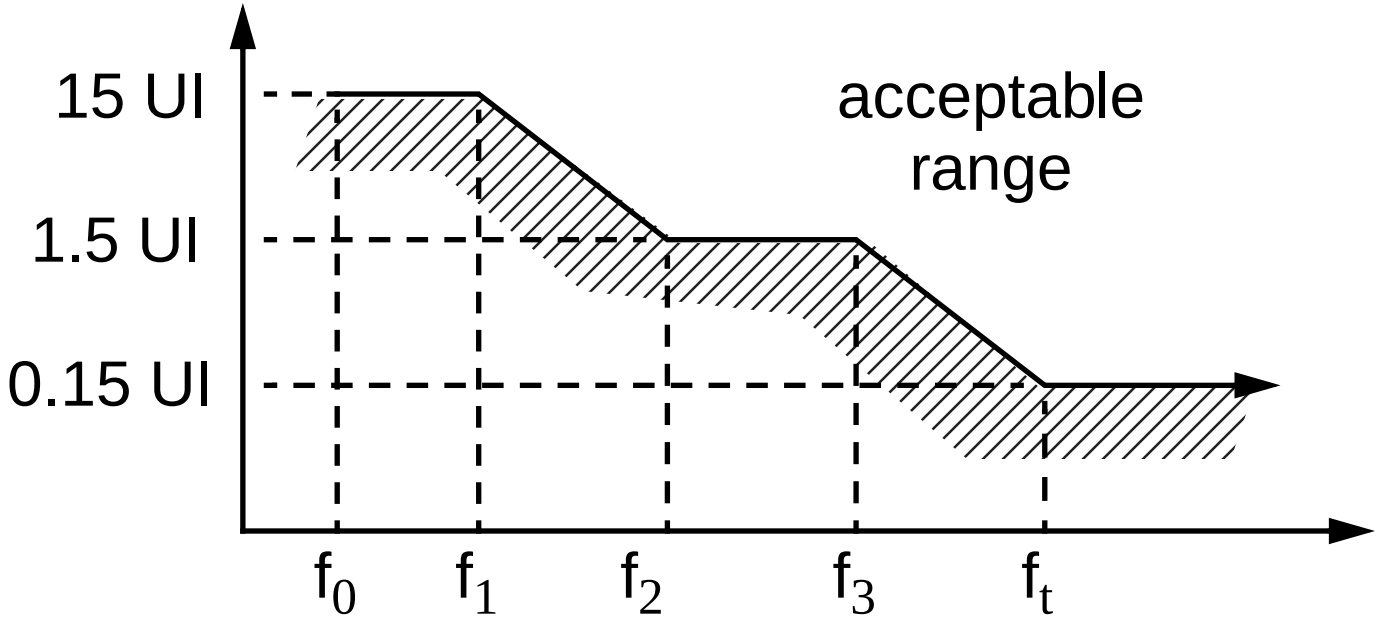
Jitter Tolerance Test Setup



At each frequency, the sinewave modulation amplitude is increased until the BER penalty is equal to that caused by 1dB optical attentuation

After Trischitta and Varma: “Jitter in Digital Transmission Systems”

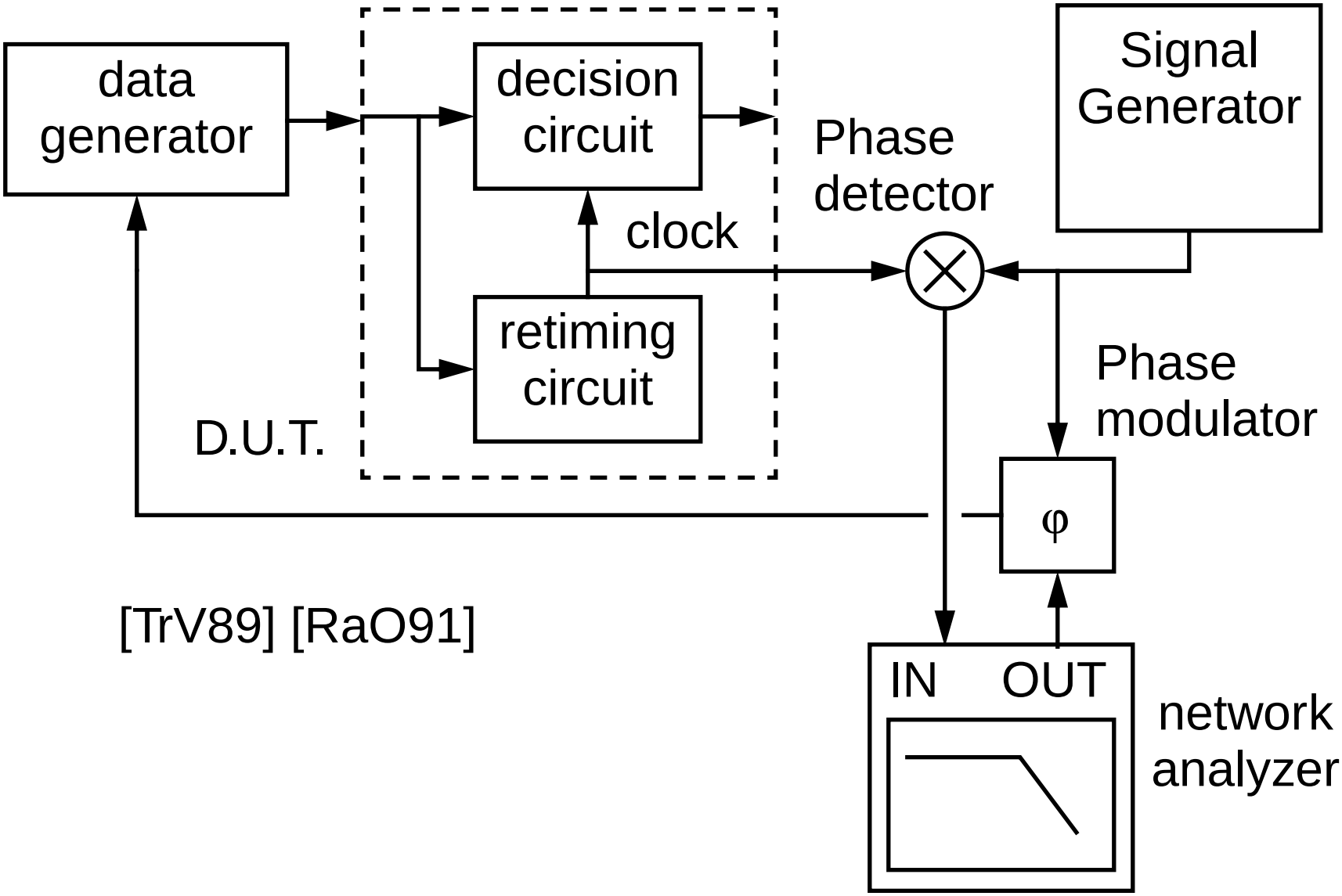
SONET Jitter Tolerance Mask



Data Rate	f_0 [Hz]	f_1 [Hz]	f_2 [Hz]	f_3 [kHz]	f_t [kHz]
155 Mb	10	30	300	6.5	65
622 Mb	10	30	300	25	250
2.488 Gb	10	600	6000	100	1000
10 Gb	?	?	?	400	4000

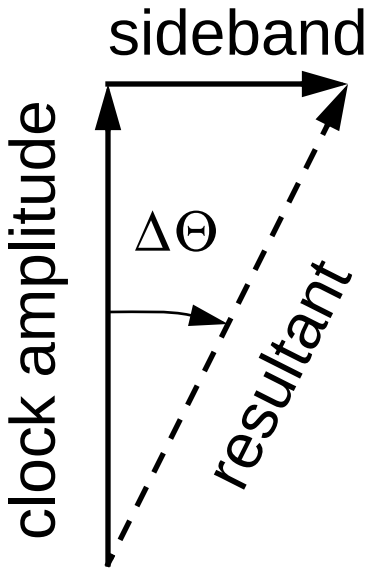
from SONET SPEC: TA-NWT-000253 Issue 6, Sept. 1990, fig 5-13

Jitter Transfer Measurement



[TrV89] [RaO91]

Jitter Transfer Analysis



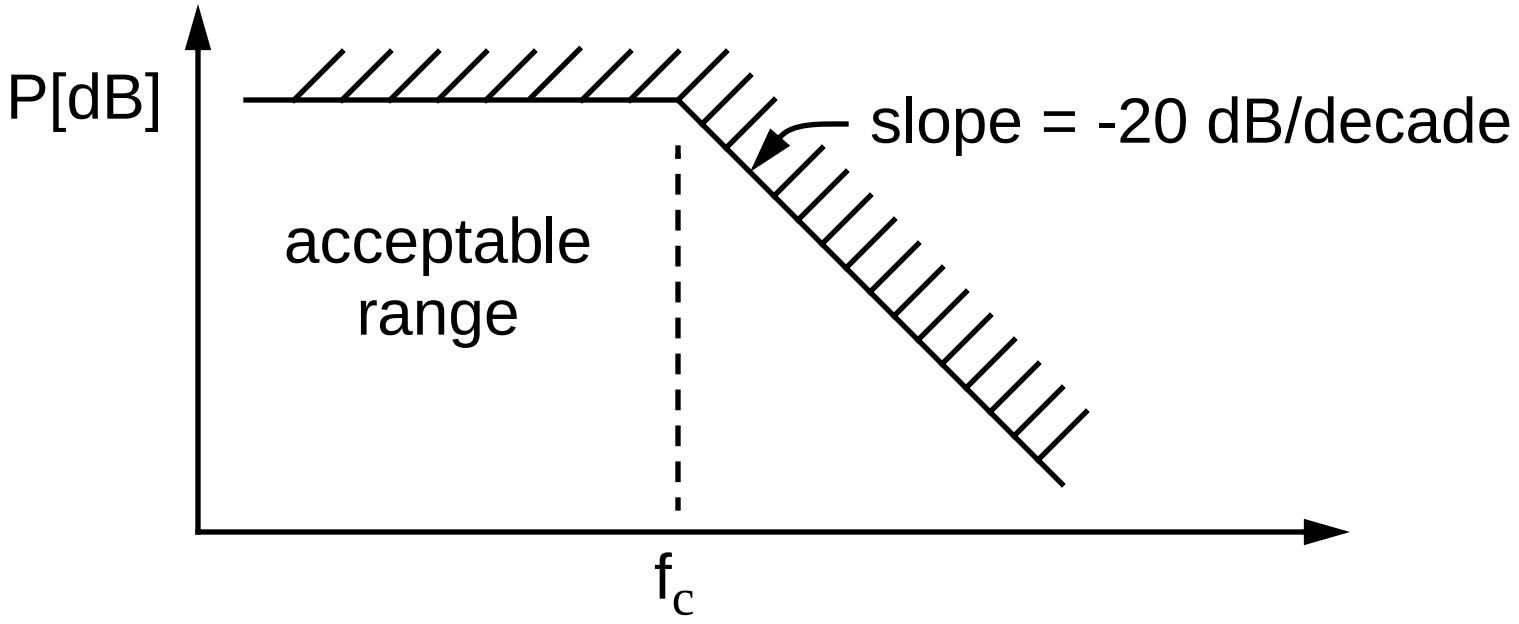
Assuming small angles (i.e.: only one dominant sideband on recovered clock):

$$Jitter_{pp(rads)} = 2\Delta\Theta \cong 2\,\mathrm{atan}\left(\frac{V_{sideband}}{V_{clock}}\right)$$

Jitter transfer is defined as the jitter at the clock output divided by the jitter at the D.U.T input, plotted as a function of jitter frequency.

??

Jitter Transfer Specification



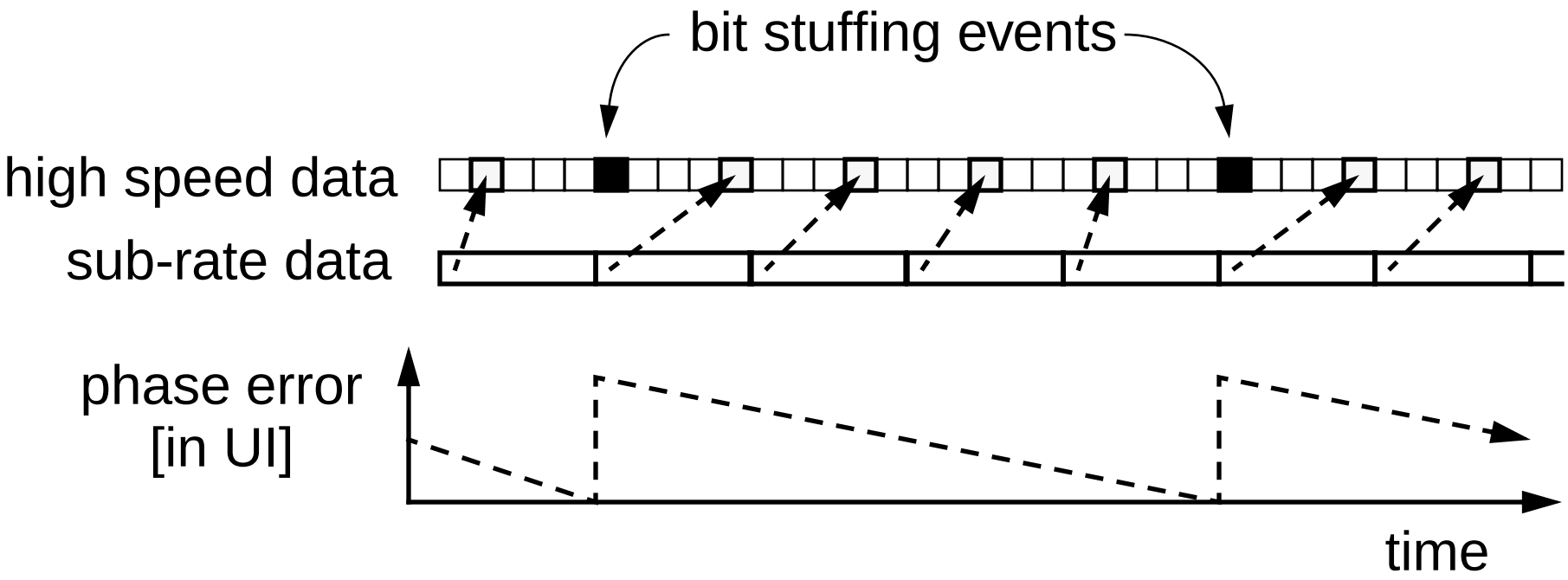
Data Rate	f_C[kHz]	P[dB]
155 Mb	130	0.1
622 Mb	500	0.1
2.488 Gb	2000	0.1

This specification is intended to control jitter peaking in long repeater chains

Some Signal Degradation Mechanisms

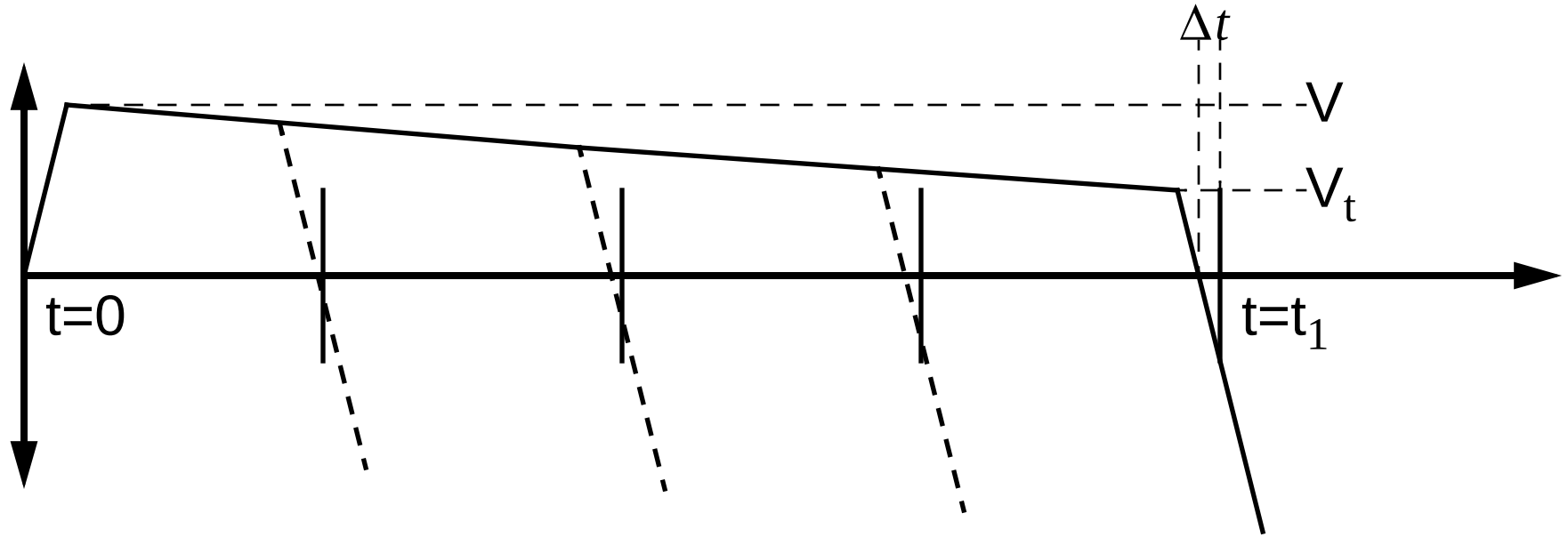
- Multiplex Jitter
- AC Coupling
- Optical Pulse Dispersion
- Skin Loss
- Random Noise
- E+O Crosstalk
- Intersymbol Interference

Multiplex Jitter



Multiplex jitter is not a problem on the high rate channel itself - it only occurs on non-synchronous, lower speed tributaries that have been sent over the high-speed channel (e.g.: DS3 over SONET OC-48).

Voltage and Time aberrations caused by AC-coupling

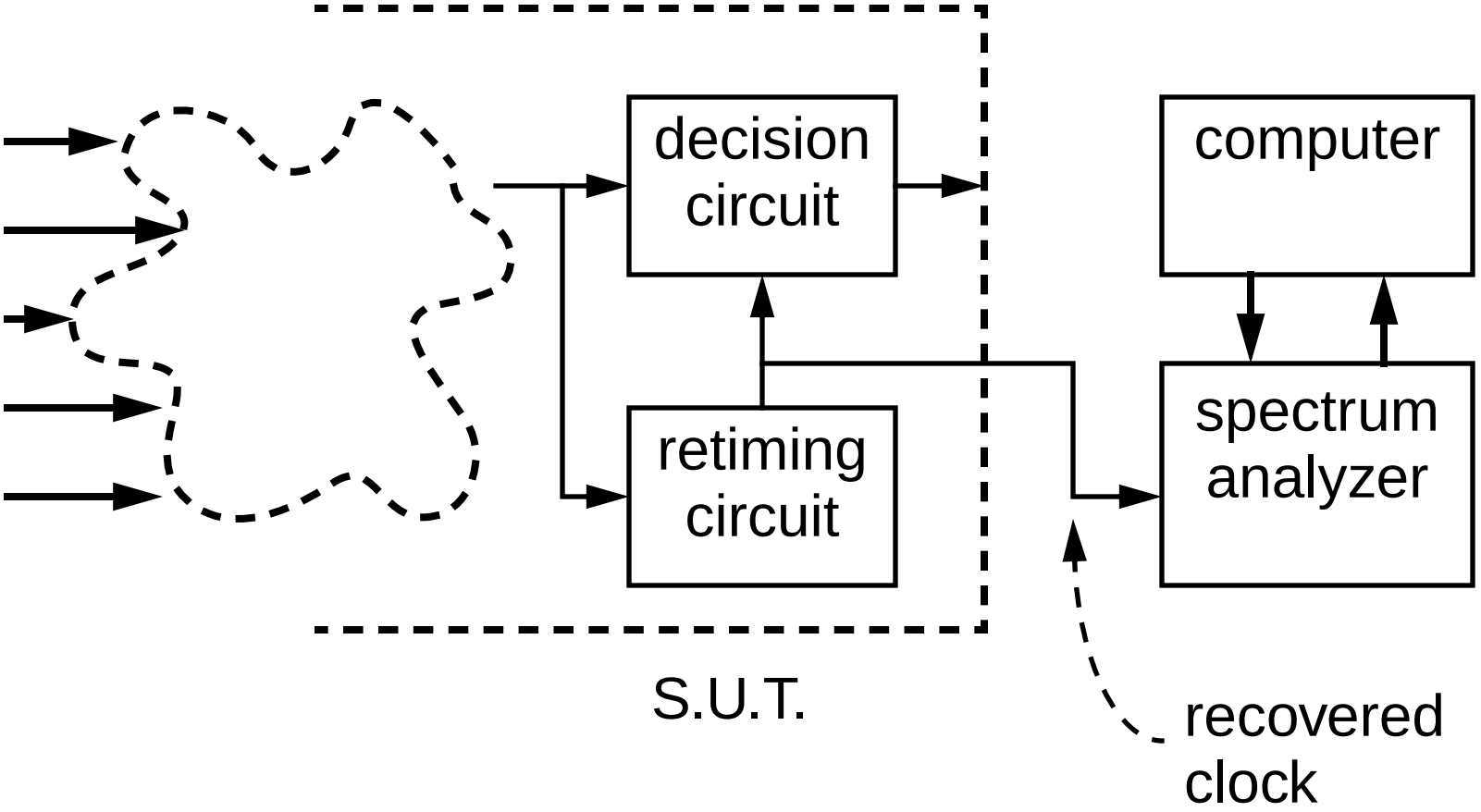


AC coupled pulses droop as $P \equiv \frac{V - V_t}{V} \times 100 \approx \frac{t_1}{RC} \times 100$.

Jitter is introduced by finite slope of pulse rise/fall time:

$$\Delta t = \frac{t_r t_1}{(2RC)}$$

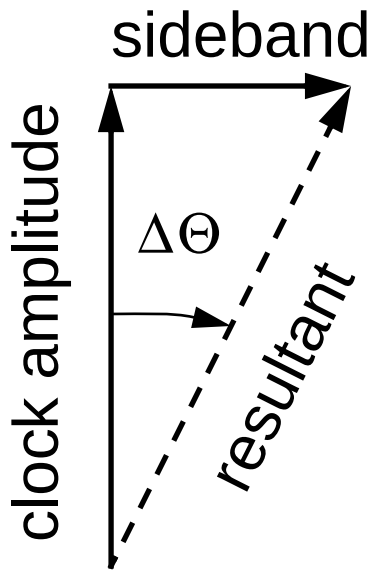
Jitter Generation



Jitter Generation (cont.)

1) Measure Jitter Sidebands around Clock

$$Jitter_{pp(rads)} = 2\Delta\Theta \cong 2\,\mathrm{atan}\left(\frac{V_{sideband}}{V_{clock}}\right)$$



2) Multiply Jitter components by Filter Mask

3) RMS sum total noise voltages over band

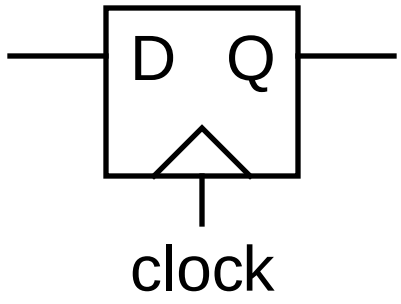
4) Convert RMS noise voltage to RMS jitter

OC-48 (2.488 Gb/s SONET) specifies 12 kHz hipass filter, and maximum 0.01 UI RMS integrated jitter.

Decision Circuit

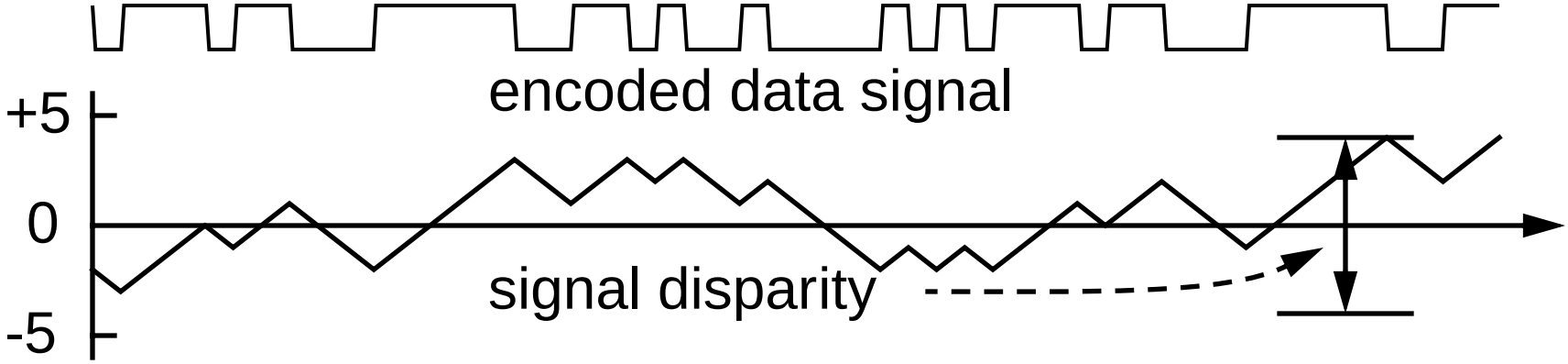
- Quantizes amplitude at precise sample instant
- Typically uses positive feedback to resolve small input signals
- A master/slave D-flip-flop carefully optimized for input sensitivity and clock phase margin is a common choice
- Latches input data on rising *edge* of clock signal

simplified schematic symbol:



Code Disparity

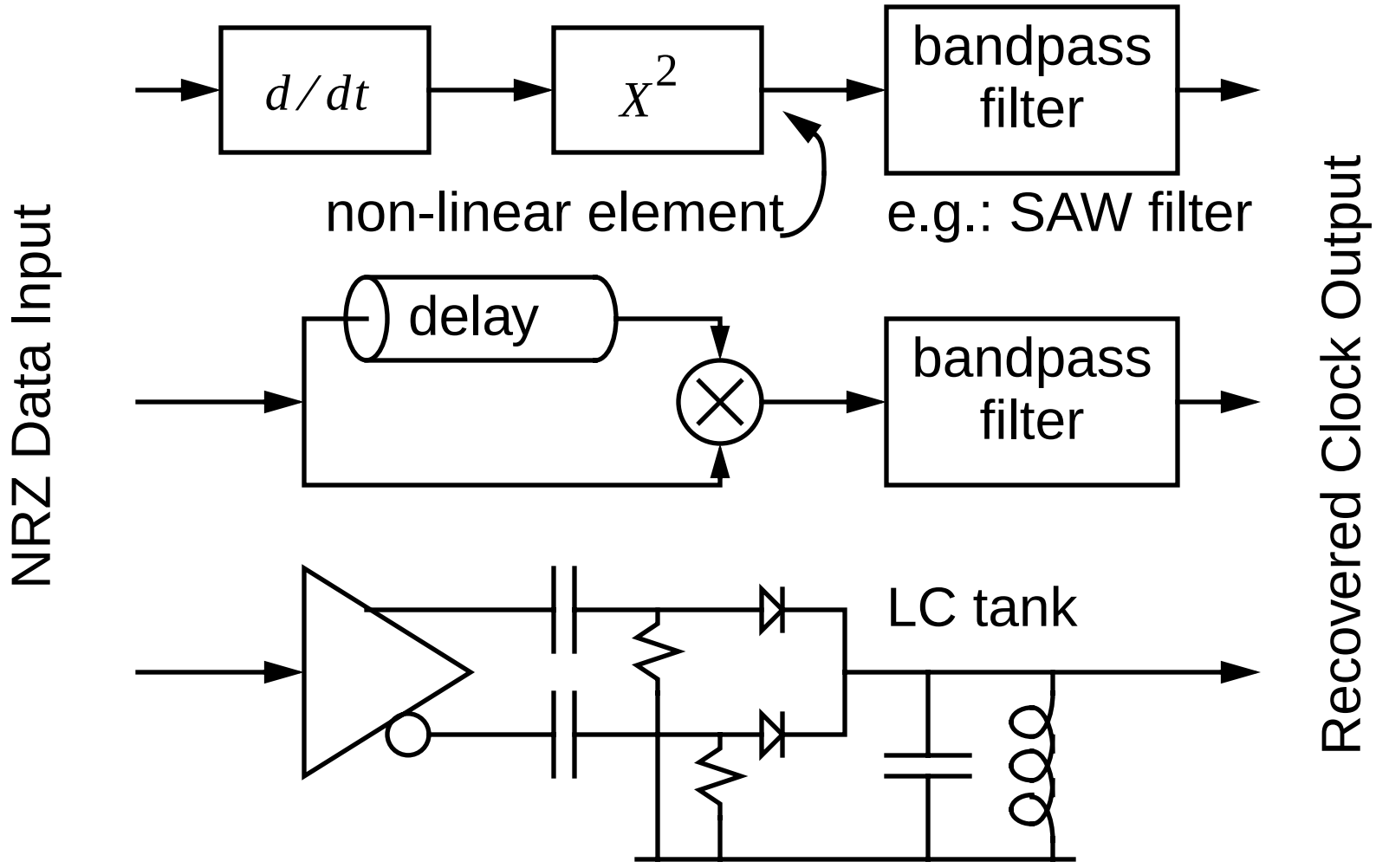
Disparity is defined as N_{high} - N_{low} in past transmitted signal



- In an *unbalanced* code the disparity can grow without limit. e.g.: 4B5B code of FDDI
- In a *balanced* code, the disparity is limited to a finite worst case value. e.g.: 8B10B of FibreChannel

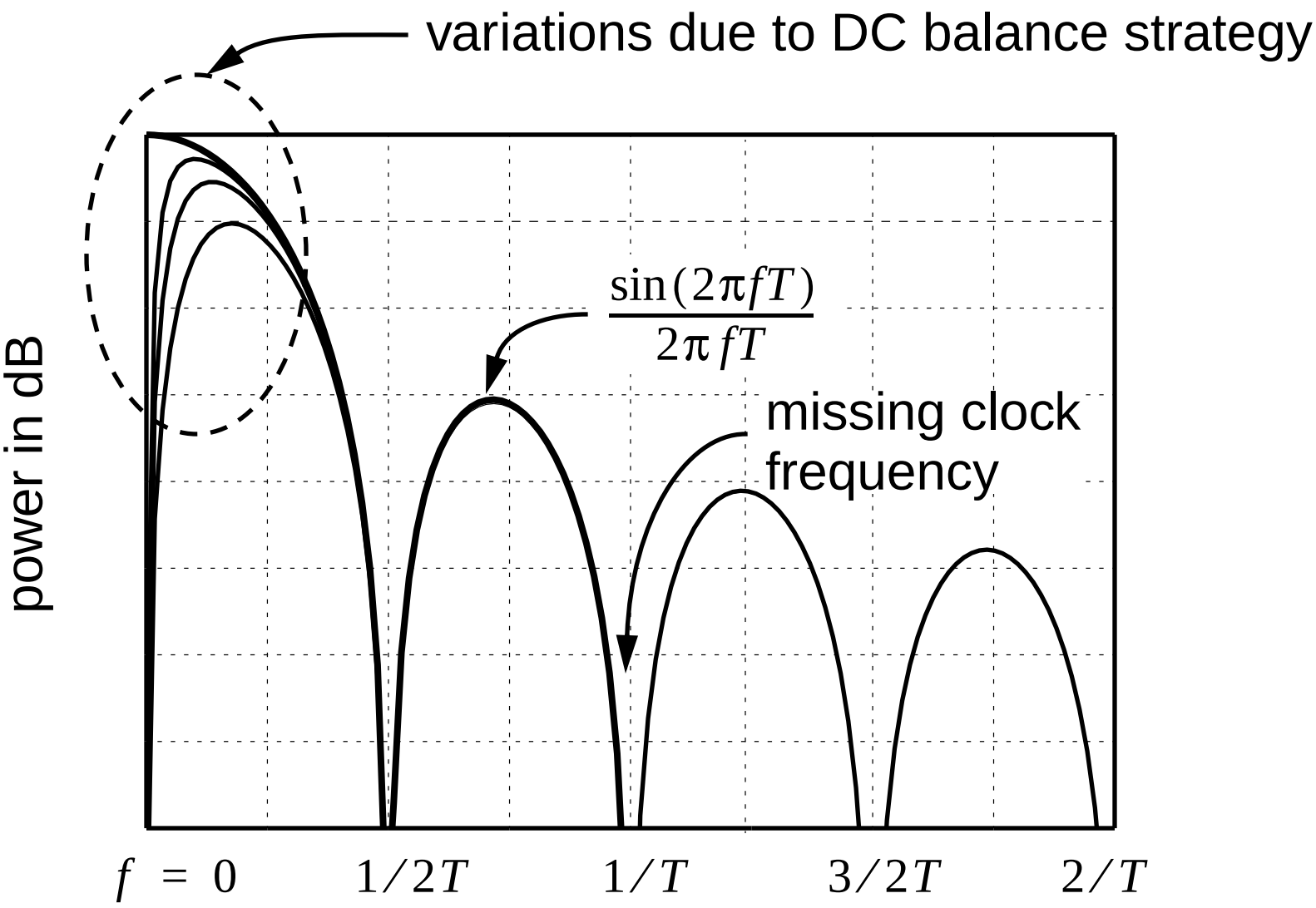
After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

Filter Method Examples



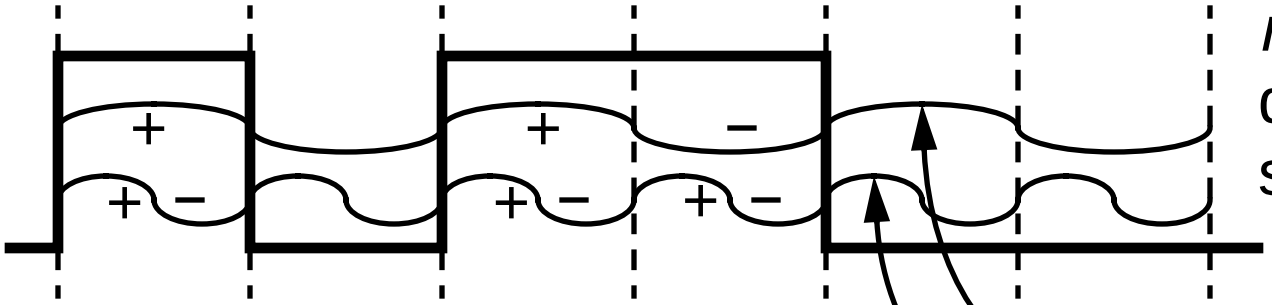
(this last circuit can be thought of as an NRZ-RZ converter)

Spectrum of NRZ data



NRZ and RZ signalling

NRZ = “non return to zero” data

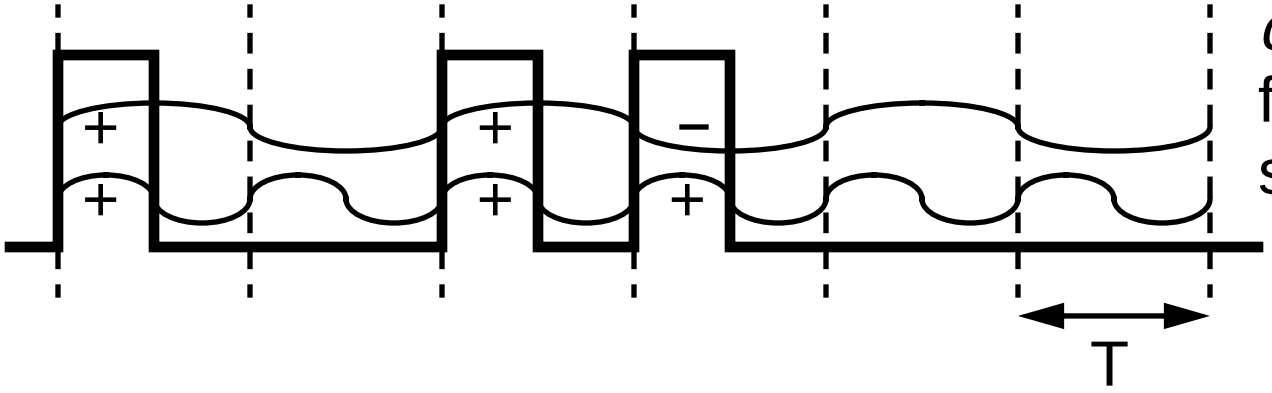


neither clock *nor* data frequency in spectrum

data frequency

clock frequency

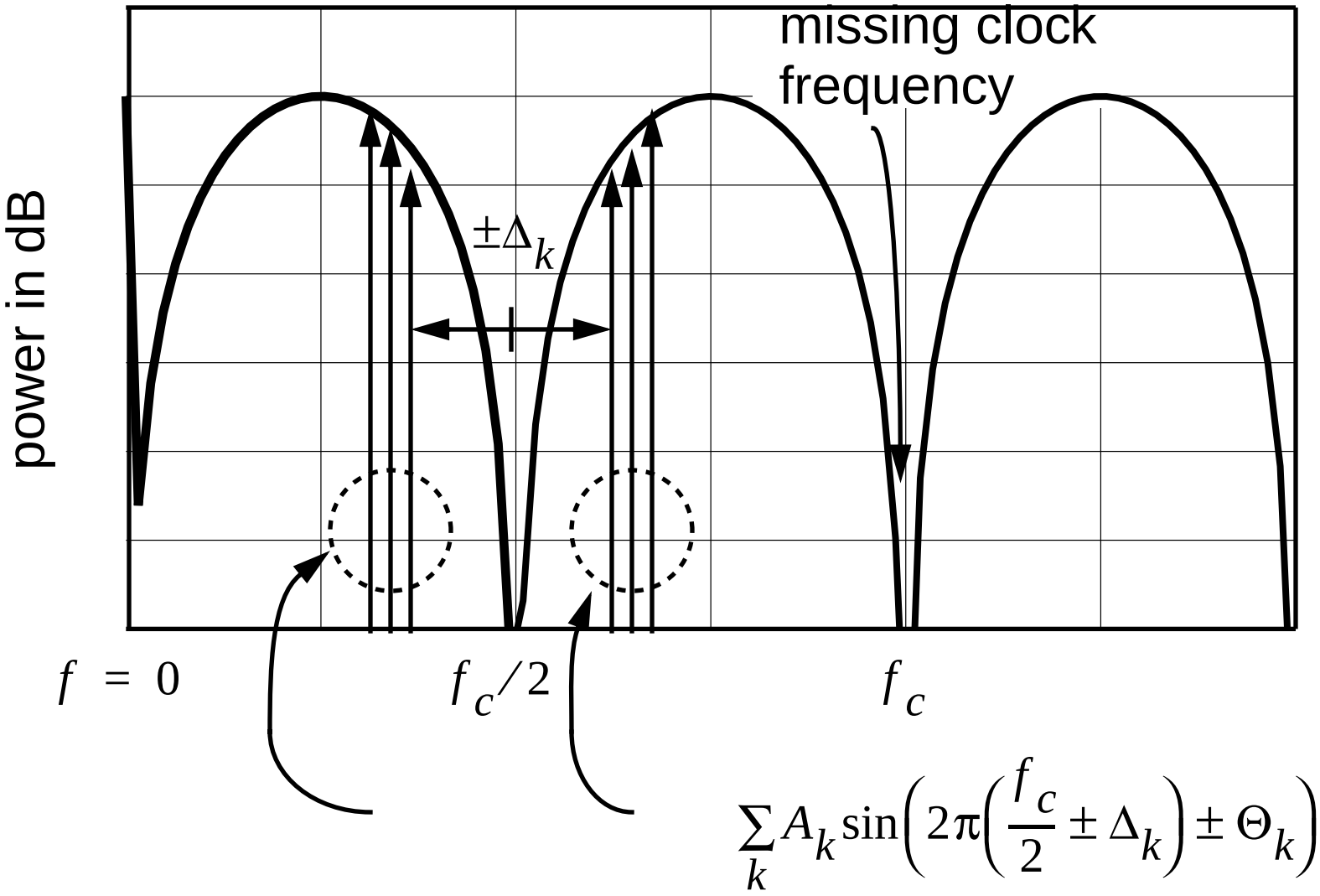
RZ = “return to zero” data



clock, but *no* data frequency in spectrum

NRZ signalling is almost universally used.

A detailed look at the spectrum of differentiated NRZ



Reconstructing the Clock

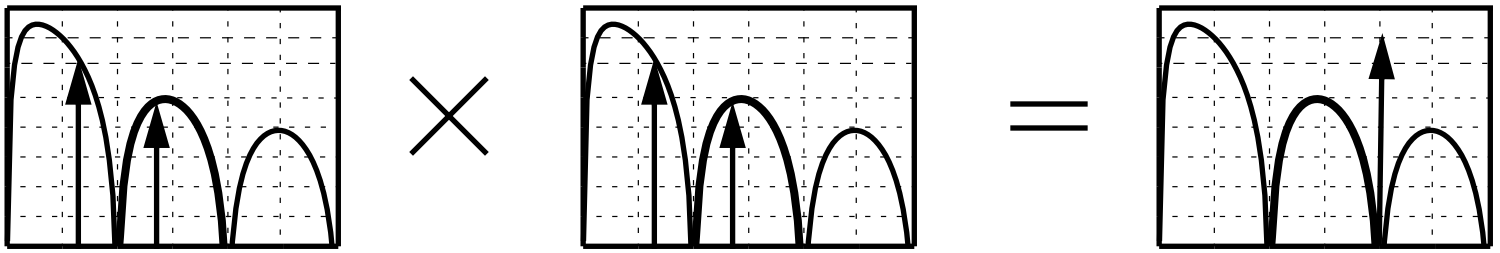
- Start with symmetric sideband pairs about $f_c/2$:

$$\sum_k A_k \sin\left(2\pi\left(\frac{f_c}{2} \pm \Delta_k\right) \pm \Theta_k\right)$$

- Mix data signal with itself (e.g.: square law):

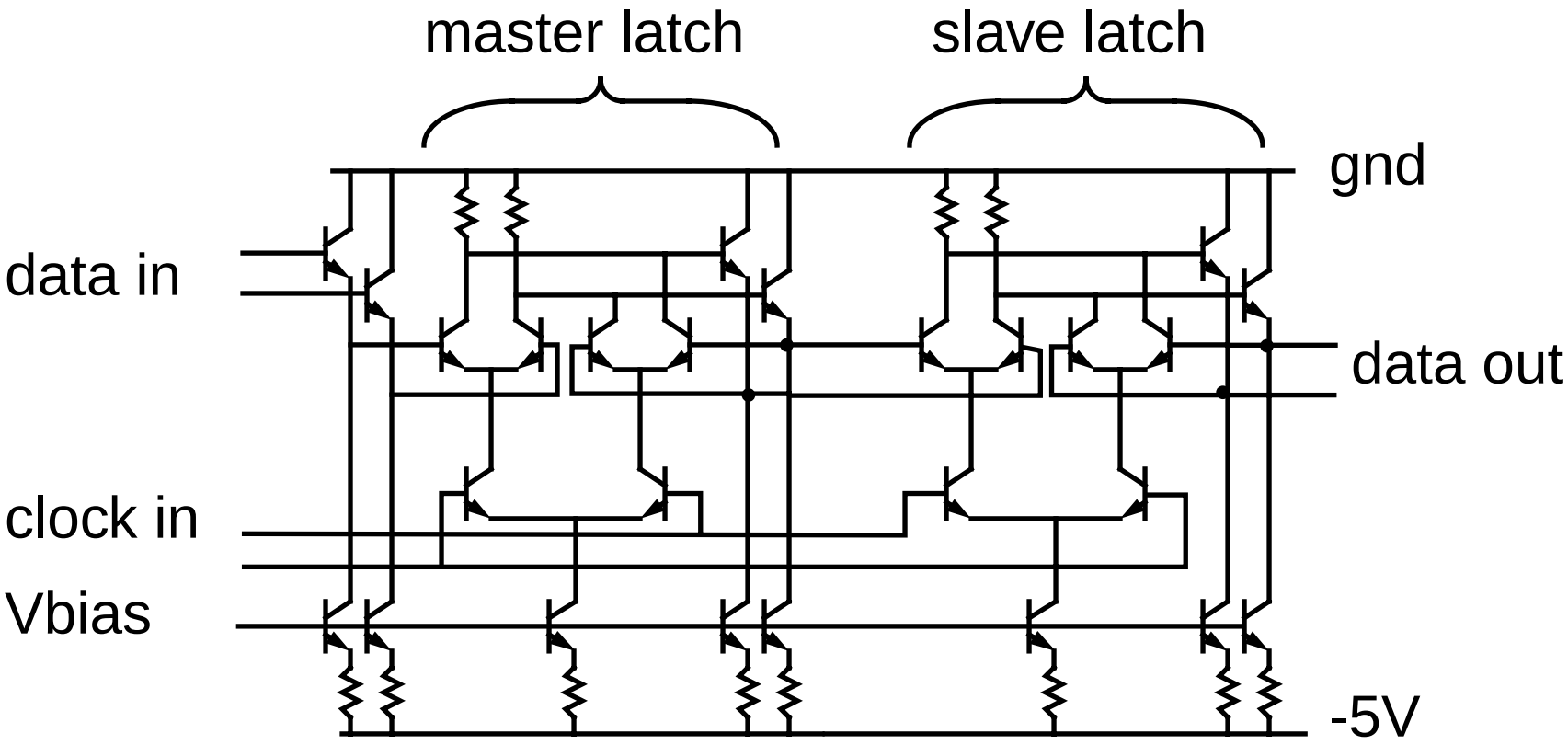
$$\sin\alpha \sin\beta = \frac{1}{2}\left[\cos(\alpha - \beta) - \cos(\alpha + \beta)\right]$$

- All the symmetric sidebands mix pairwise to coherently create a carrier frequency component:



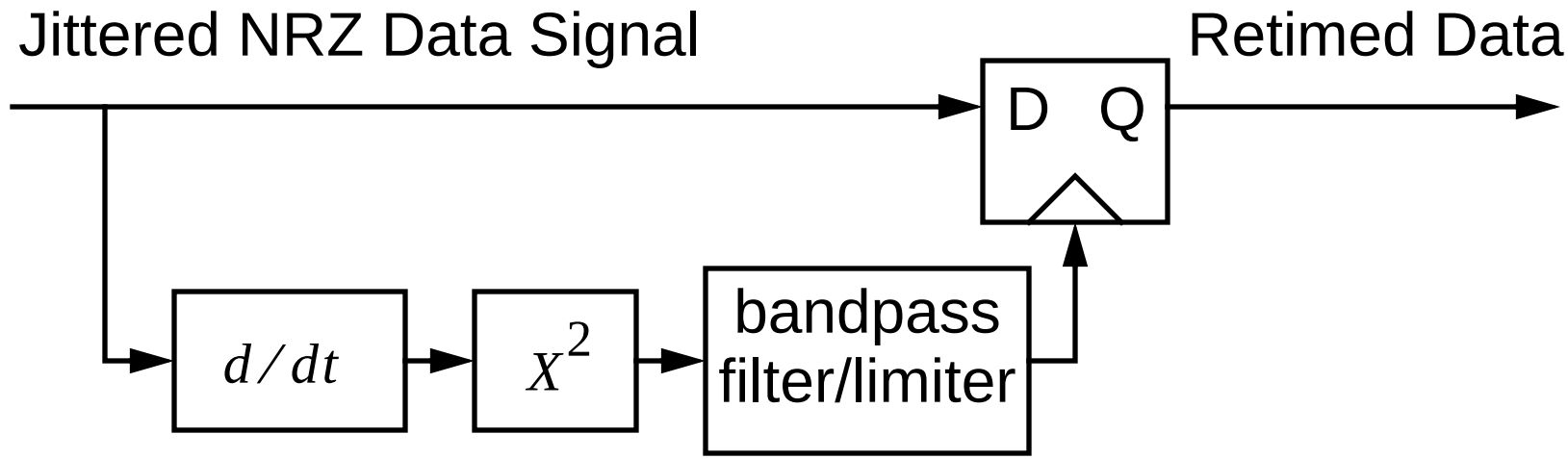
direct implementation of this principle is “Filter Method”

Example Bipolar Decision Circuit



- many clever optimizations are possible

Summary of Filter Method



Pro:

Very simple to implement

Can be built with microwave “tinkertoys” using coax to very high frequencies

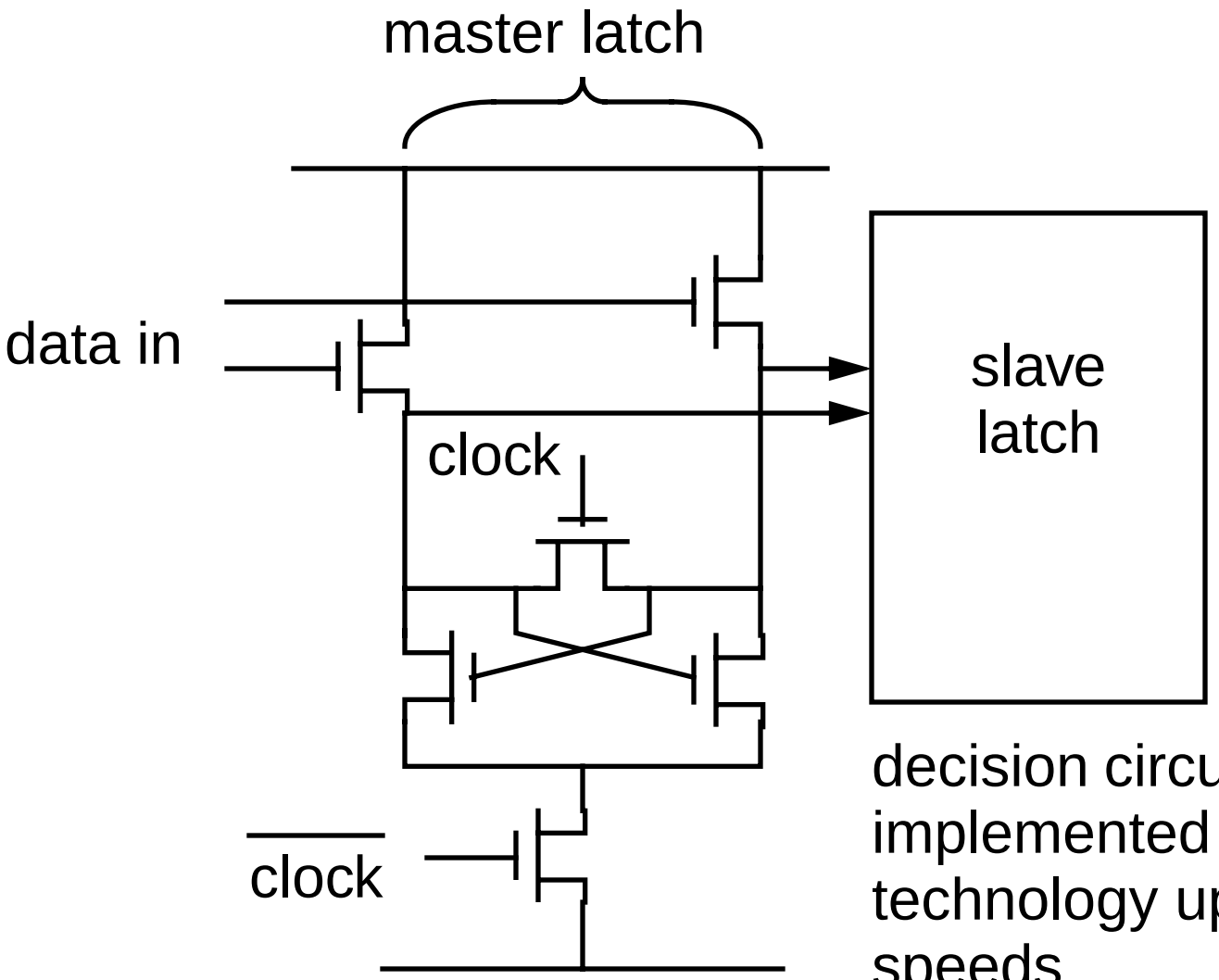
Con:

Temperature and frequency variation of filter group delay makes sampling time difficult to control

Narrow pulses imply high f_T

Hi-Q filter difficult to integrate

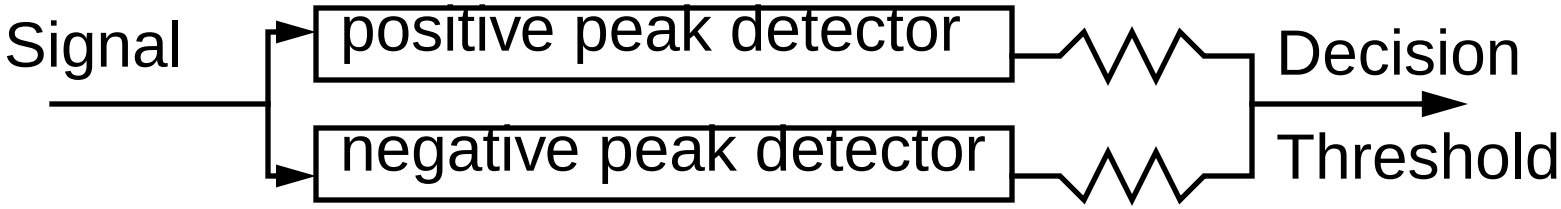
Example MOS Decision Circuit



decision circuits can be implemented in NMOS technology up to Gb/s speeds

Decision Threshold Generation

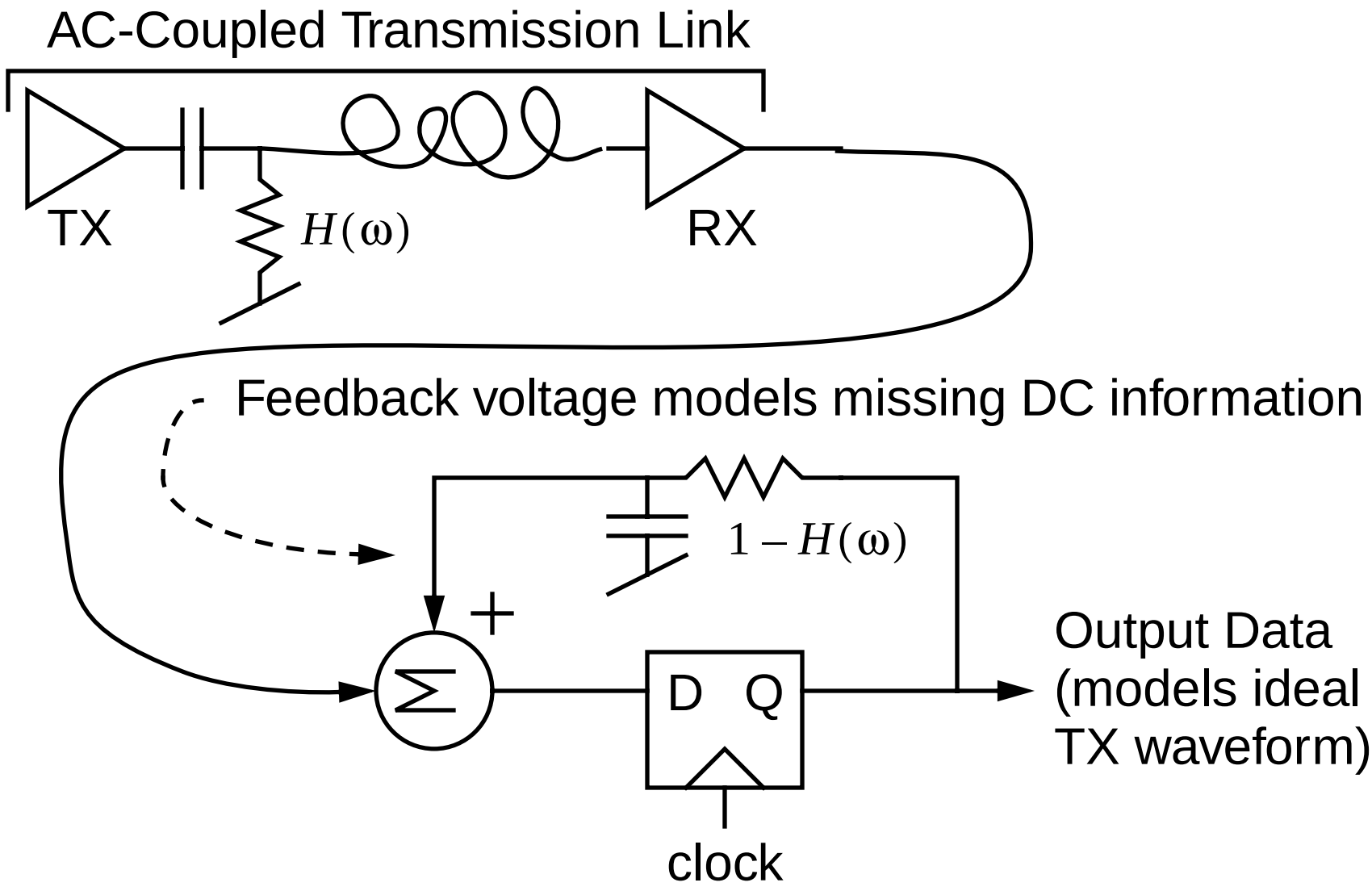
- To minimize bit-error rate, the decision threshold X-X must centered in the signal swing. Two common ways of automatically generating threshold voltage are:
  - Peak detection of signal extremes, limited run-length required



  - Decision threshold = signal average, balanced signal required

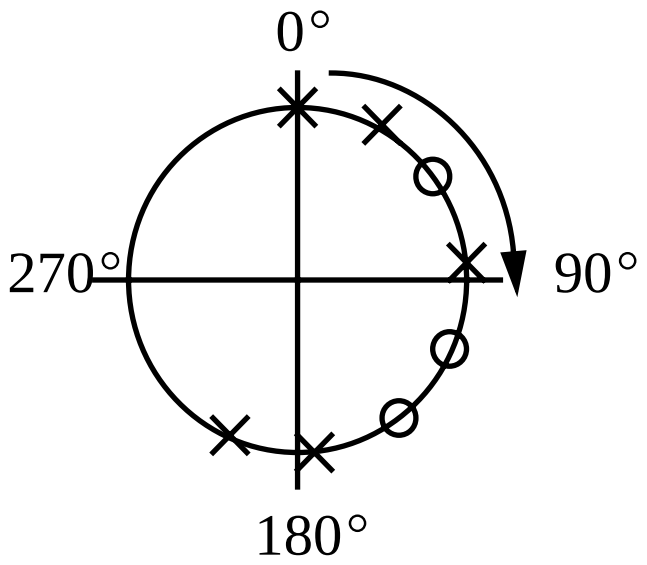
After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

Quantized Feedback



Phasor Diagram

- Graph of relative phase between clock and data
- Each complete rotation is 1 unit interval of phase slip
- Rotations/second = frequency error (in Hz)



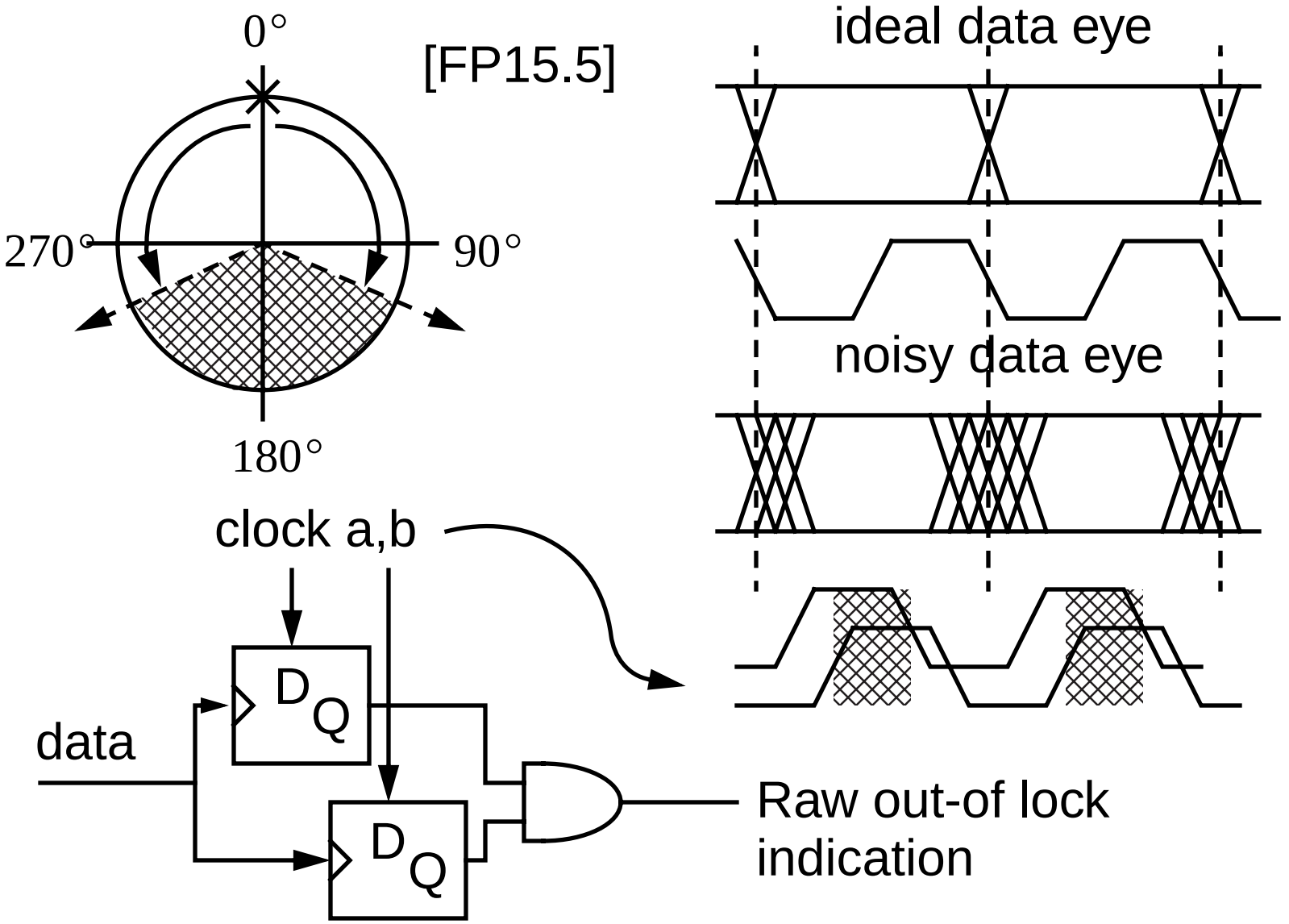
Plot of data transitions versus VCO clock phase.

Data at 1/2, or VCO at 2x, the proper frequency look locked. This puts a limit on VCO tolerance to prevent false locking.

○ = missing transitions

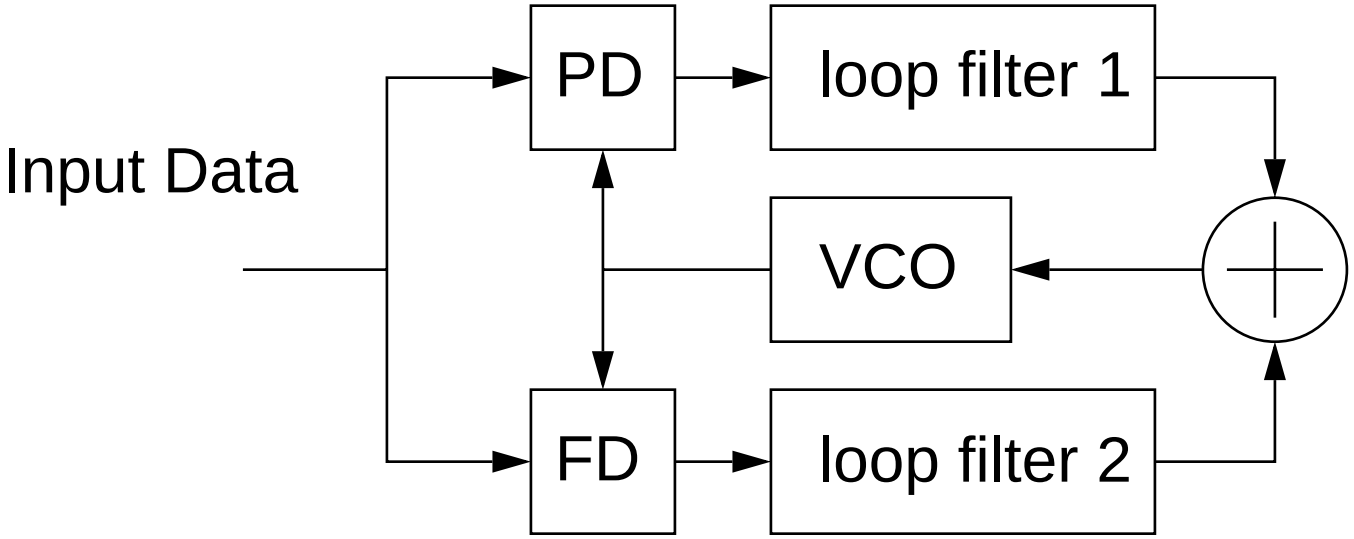
× = actual transitions

Example Lock Detector



Aided Acquistion

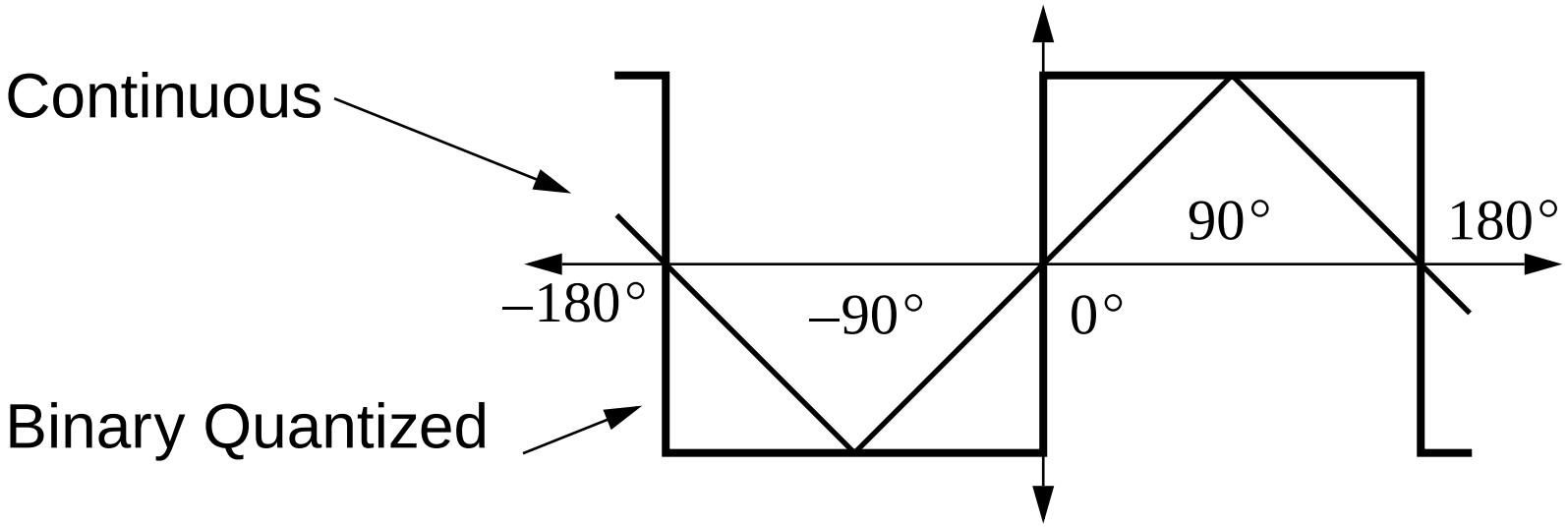
- Tricky task due to Nyquist sampling constraints caused by stuttering data transitions



- Still subject to false lock if VCO range is too wide

Phase Detectors

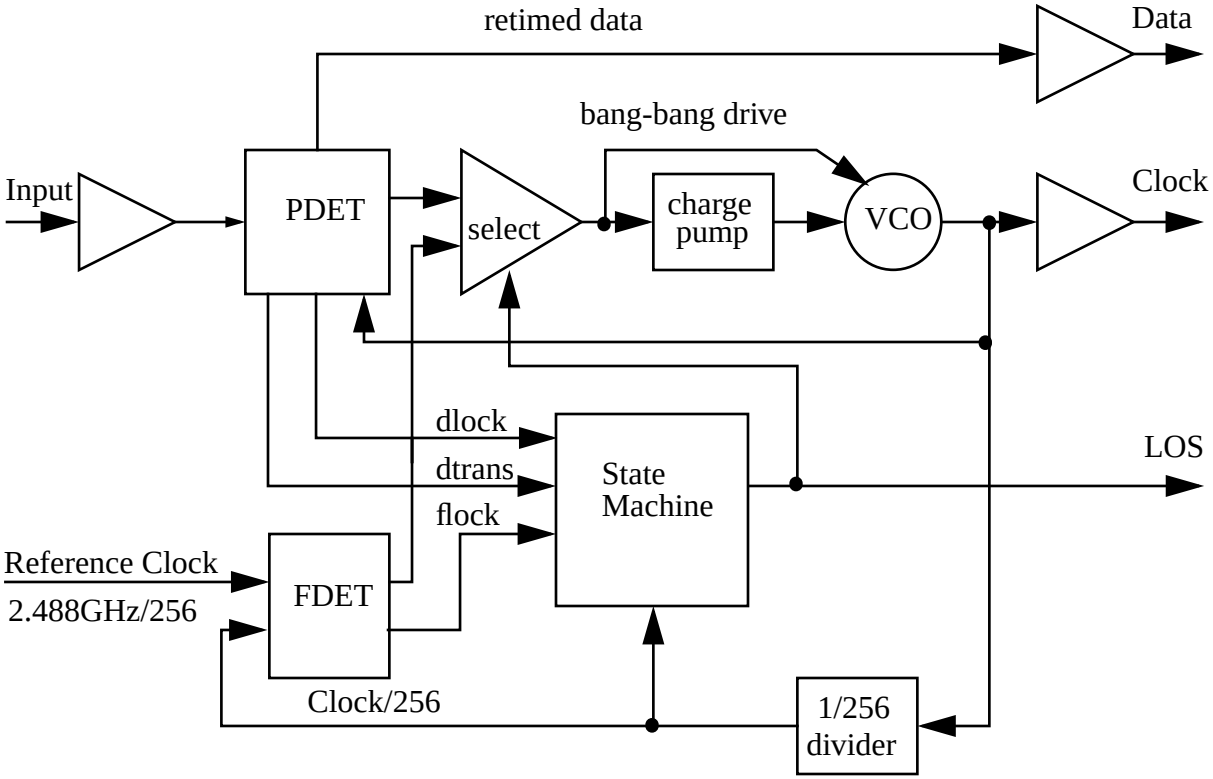
- Phase detectors generate a DC component proportional to deviation of the sampling point from center of bit-cell
- Phase detectors are:



- Binary quantized phase detectors are also called “Bang-bang” phase detectors

After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

Training Loops



An increasingly common technique is to provide a reference clock to the CDR circuit. This allows the VCO process-variation to be dynamically trimmed out, avoiding false locking problems. (Figure from paper FP15.5, 1997 ISSCC)

Coding for Desirable Properties

- DC balance, low disparity
- Bounded run length
- High Coding Efficiency
- Spectral Properties (decrease HF and/or DC component)
- *Many Variations are Possible!*
  - Manchester [San82]
  - mB/nB [Gri69][Rou76][WiF83] [YKI84] [Pet88]
  - Scrambling [CCI90]
  - CIMT [WHY91]

Simple 3B/4B code example

3B Input Data	4B Output Data	
	Even Words	Odd Words
000	0011	
001	0101	
010	0110	
011	1001	
100	1010	
101	1100	
110	0100	1011
111	0010	1101
SyncA	0111	1110
SyncB	1000	0001

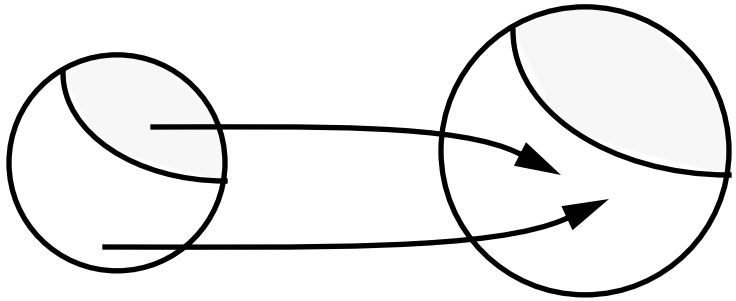
Maximum Runlength is 6

Coding Efficiency is 4/3

Sending Sync Sequence:

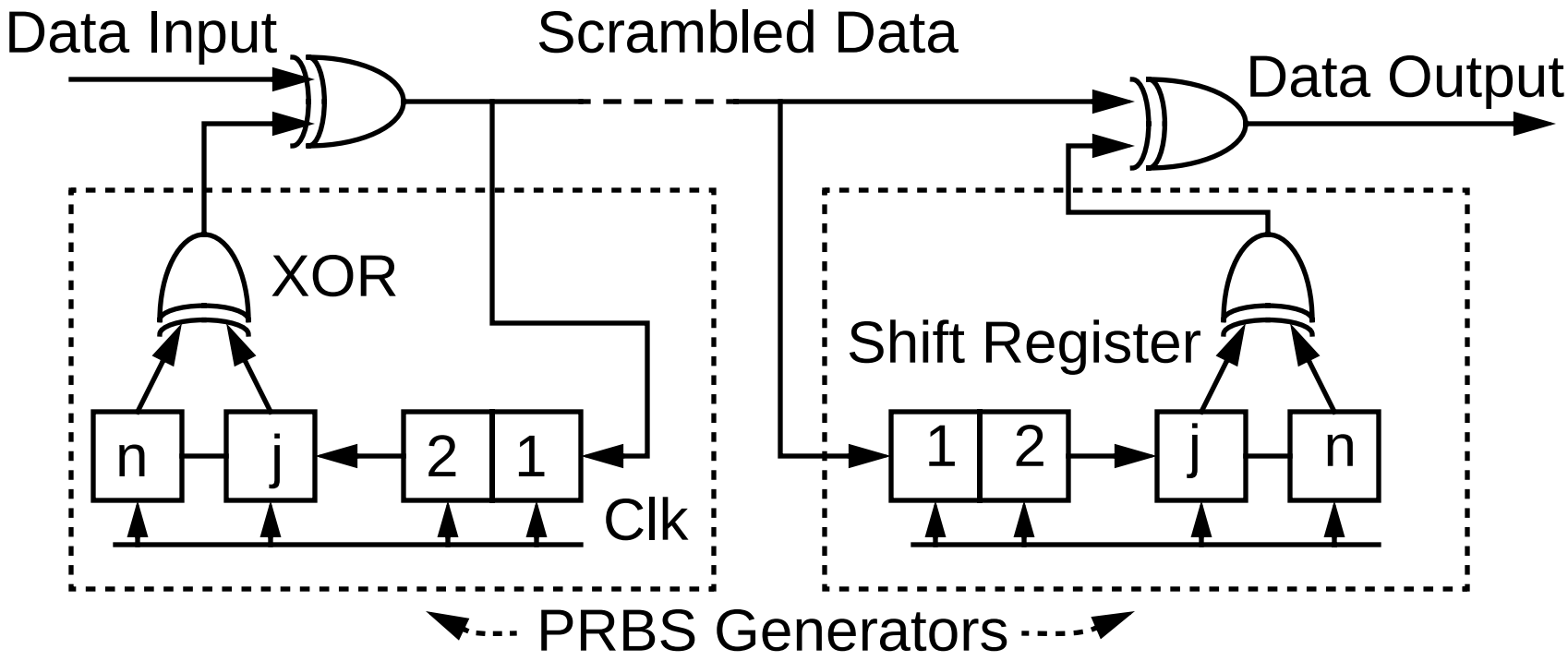
SyncA(even), SyncA(odd), SyncB(even), SyncB(odd)

allows the unambiguous alignment of 4-bit frame

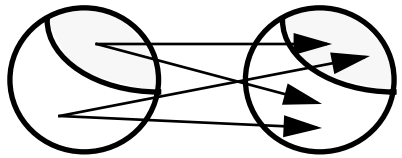


Scrambling

- Uses a feedback shift register to randomize data - reversing process at receiver restores original data



Caveat: Only guarantees balance and run-length under very specific data conditions!



After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

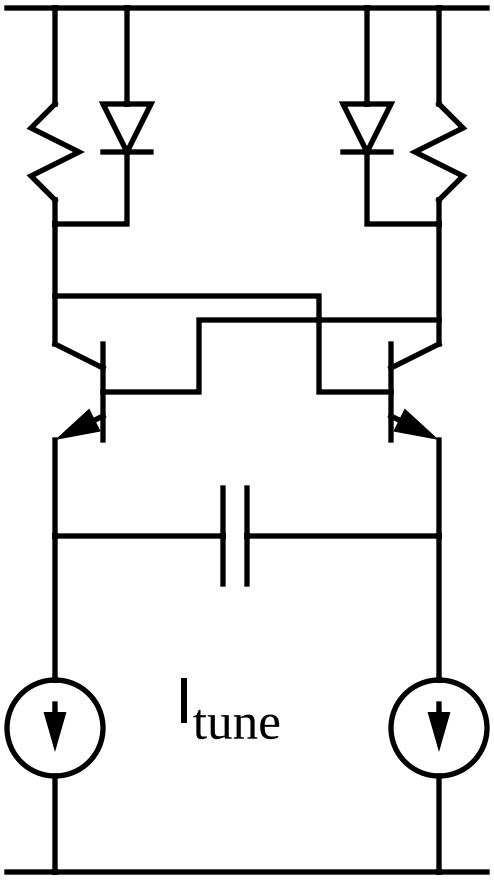
VCO alternatives

	LC Oscillator	Multivibrator	Ring Oscillator
Speed	Technology Dependent 1-10's of GHz, CMOS 1-2 GHz		
Phase Noise	Good	Poor	
Integration	Poor (L, Varactor)	Excellent	
Tunability	Narrow/Slow	Wide/Fast	
Stability	Good	Poor (needs acquisition aid)	
Other			Multi-Phase Clocks

- [Cor79, Ena87, Wal89, DeV91,Lam93, WKG94]

After Todd Weigandt, B. Kim, P.Gray, "Timing Jitter Analysis for High-Frequency CMOS Ring Oscillators", March 10, 1994

Multivibrator VCO



Capacitor is alternately charged and discharged by constant current

Tuned by varying I_{tune} in current source

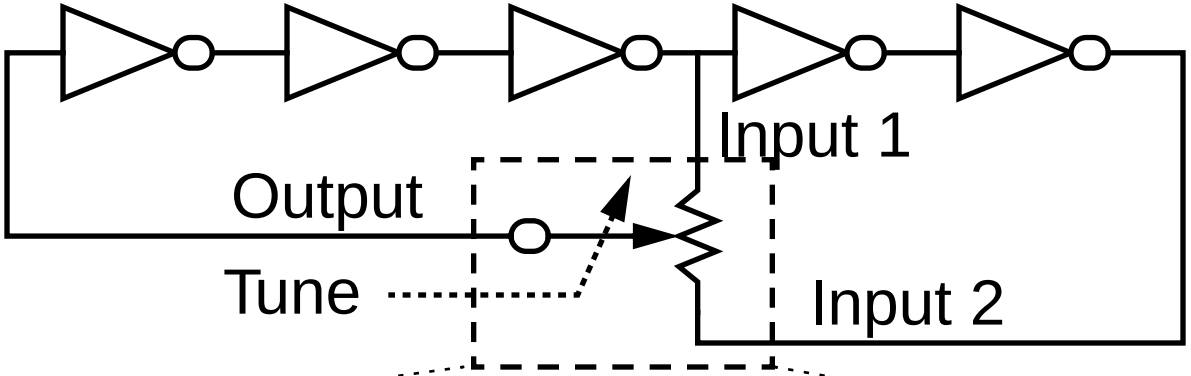
Diode clamps keep output voltage constant independent of frequency

Relies on non-linear switching for oscillation behavior, and so is limited to moderate frequencies.

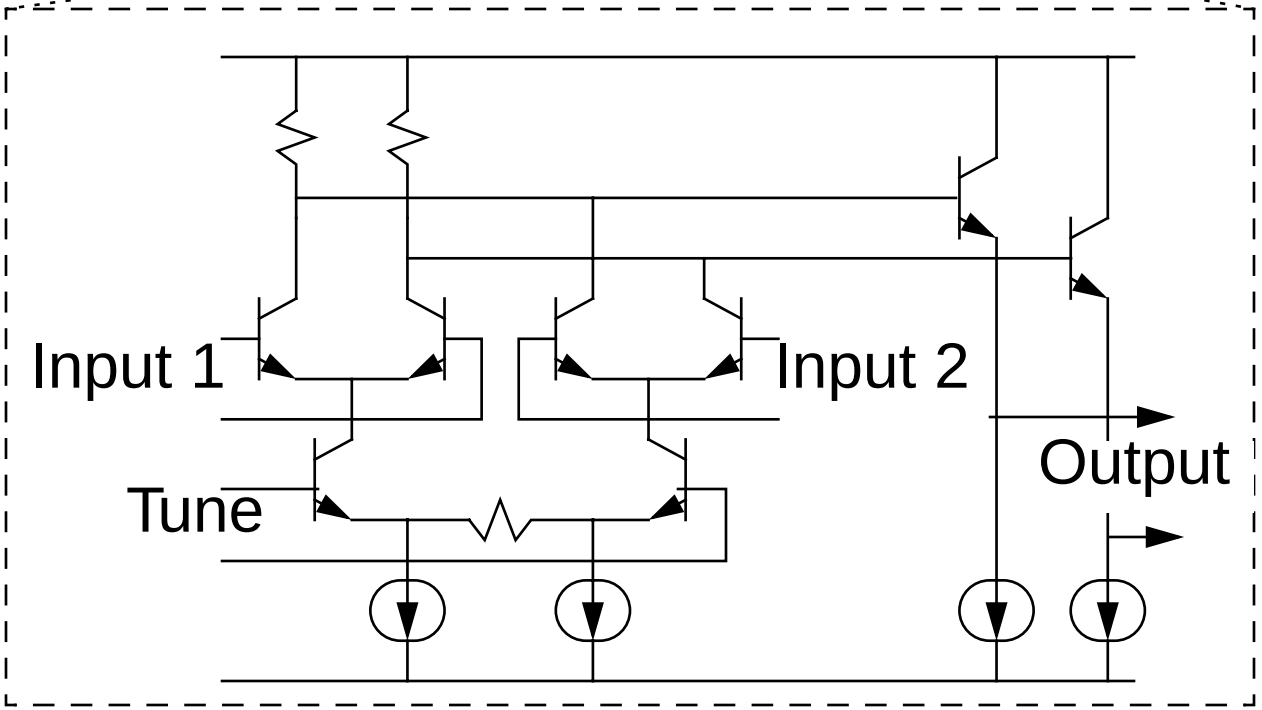
Frequency = $\frac{I_{tune}}{4CV_{be}}$

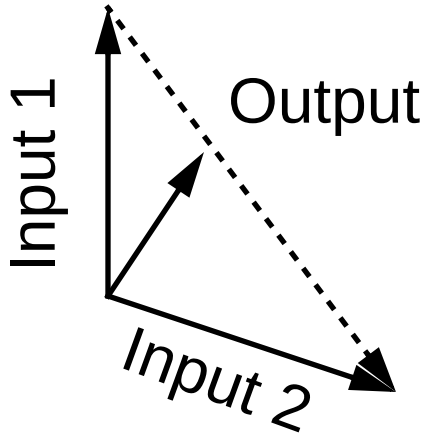
After Alan B. Grebene, “Analog Integrated Circuit Design”, Van Nostrand Reinhold, 1972, pp 313-315

Example Ring Oscillator VCO



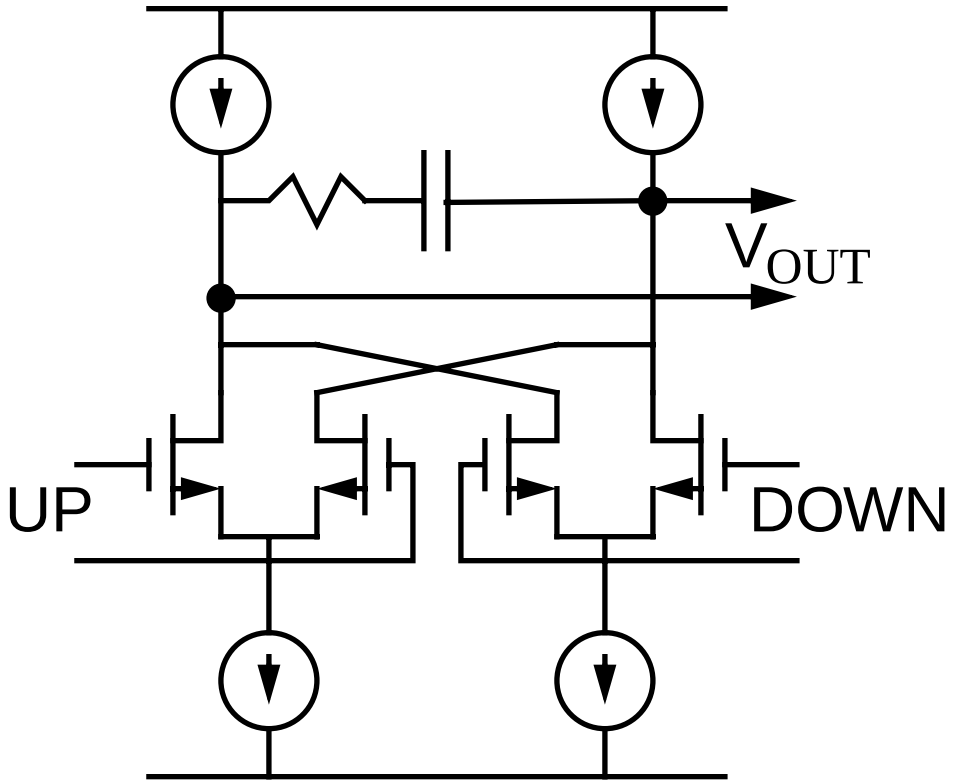
[SyA86]
[EnA87]
[Wal89]





Loop Filters

- may be analog (integrator) or digital (up-down counter)
- should have provision for holding value constant (tri-stating) under long run-length conditions

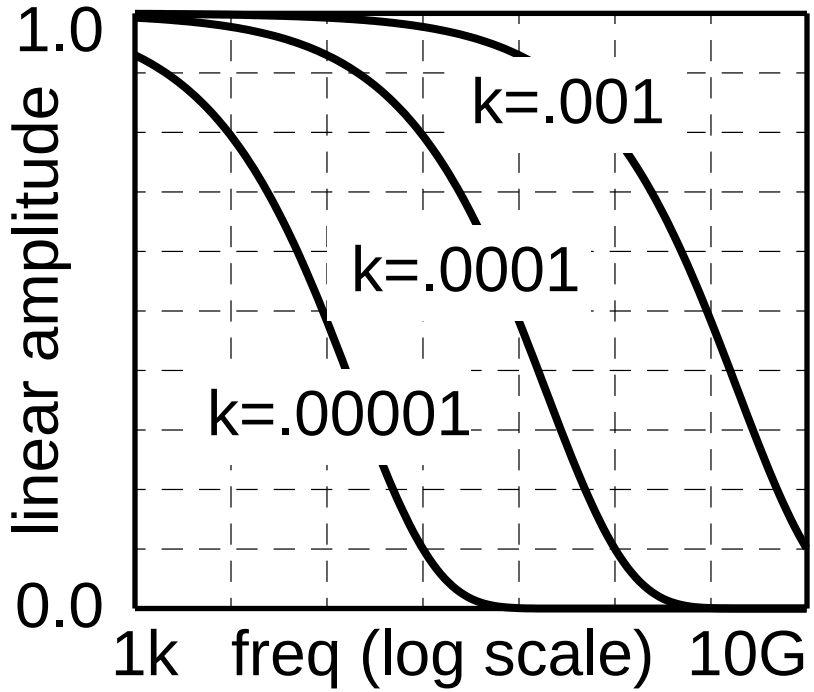


[Den88] [Dev91]
[LaW91] [WuW92]

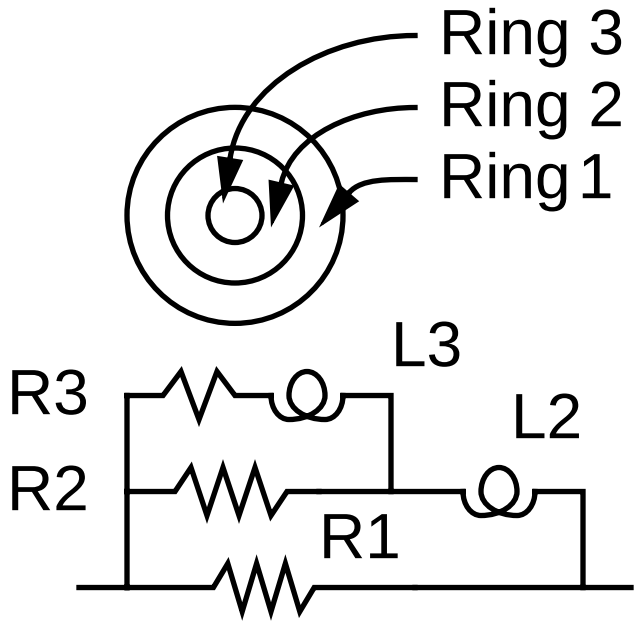
UP	DOWN	V_{OUT}
0	0	tristate
0	1	ramp DOWN
1	0	ramp UP
1	1	tristate

Skin Loss

- Nearly all cables can be modeled by the Skin Loss Equation with various k factors: $T(f) = 10^{(-k)\sqrt{f}}$.

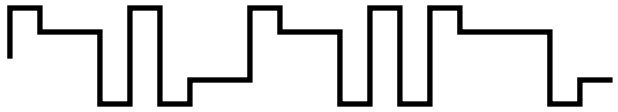


[YFW82]

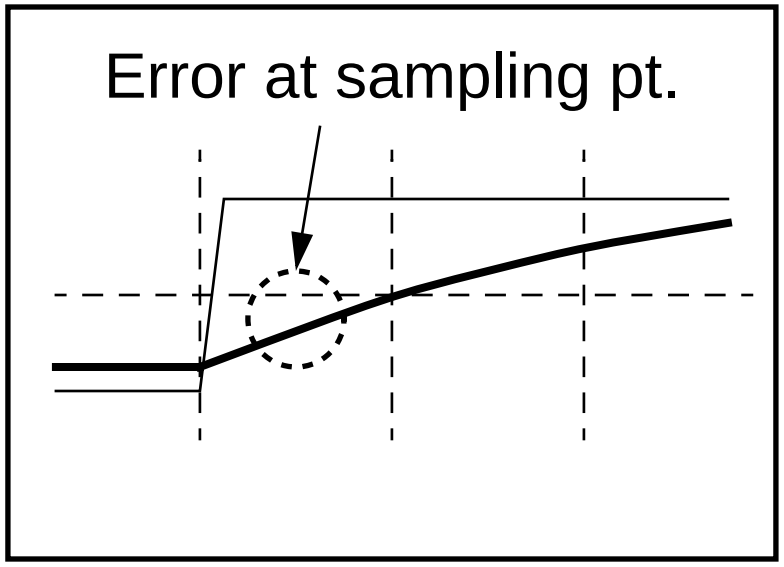


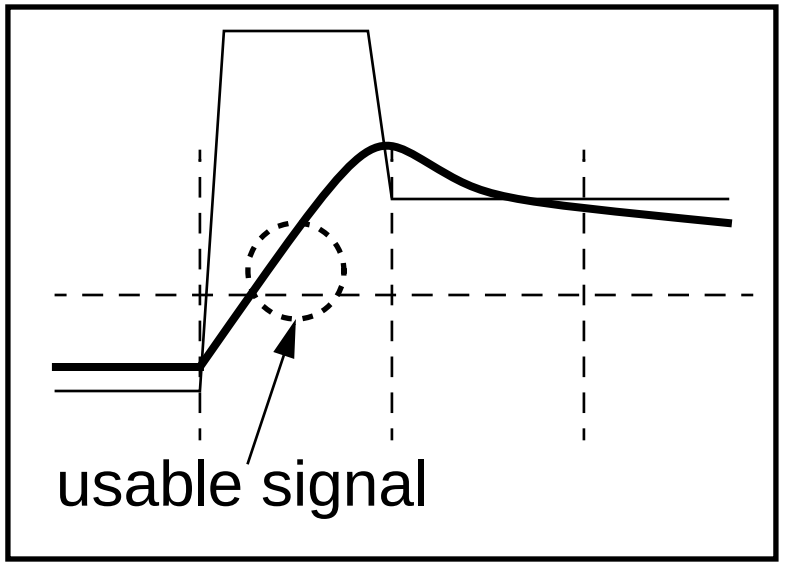
Three-element equivalent circuit of a conductor with skin loss

Skin Loss Equalization at Transmitter

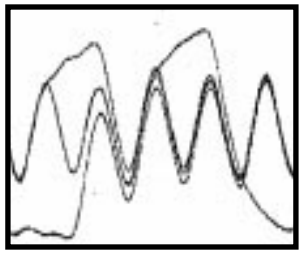


boost the first pulse after every transition

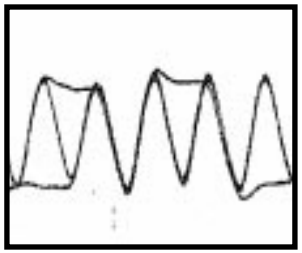




See Paper:
FP15.1, 1997
ISSCC

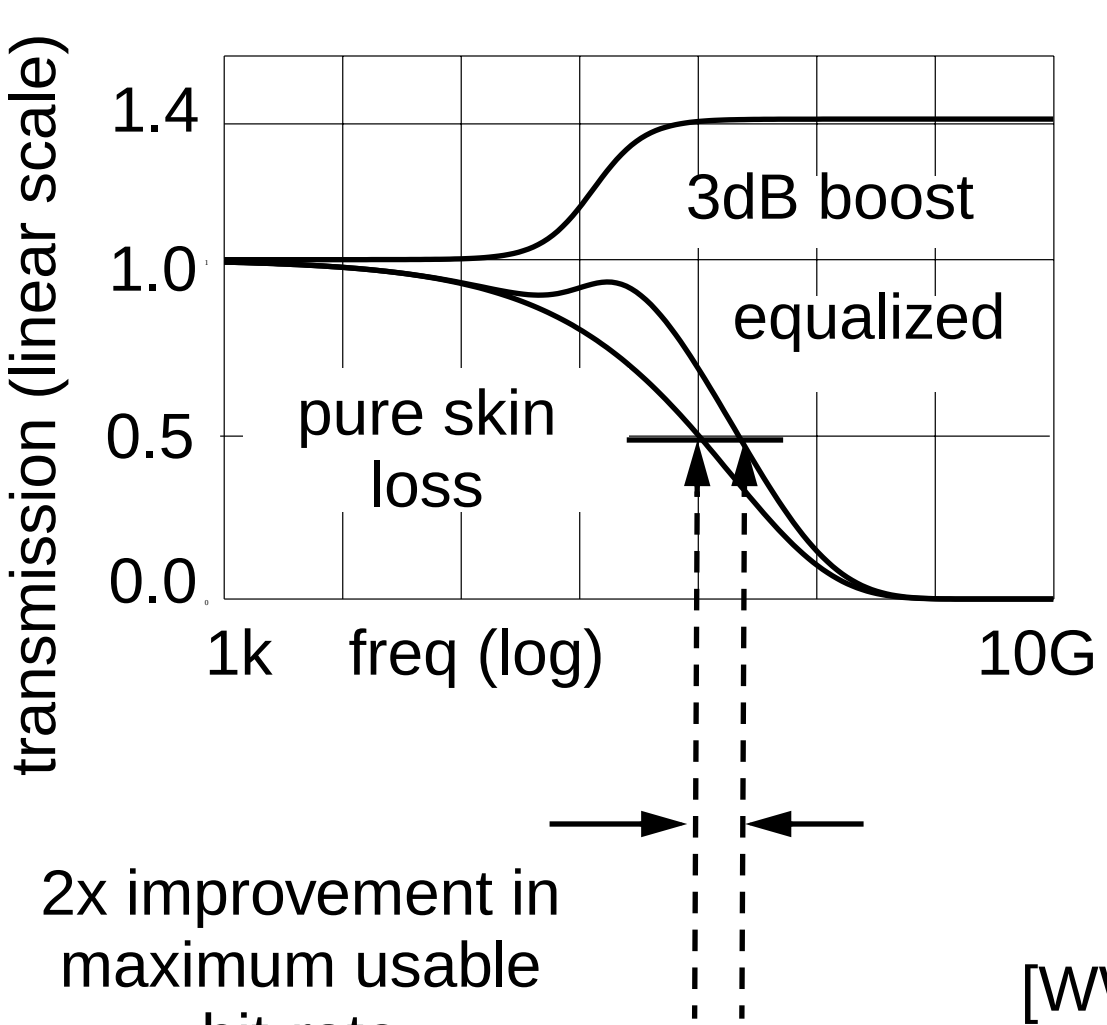


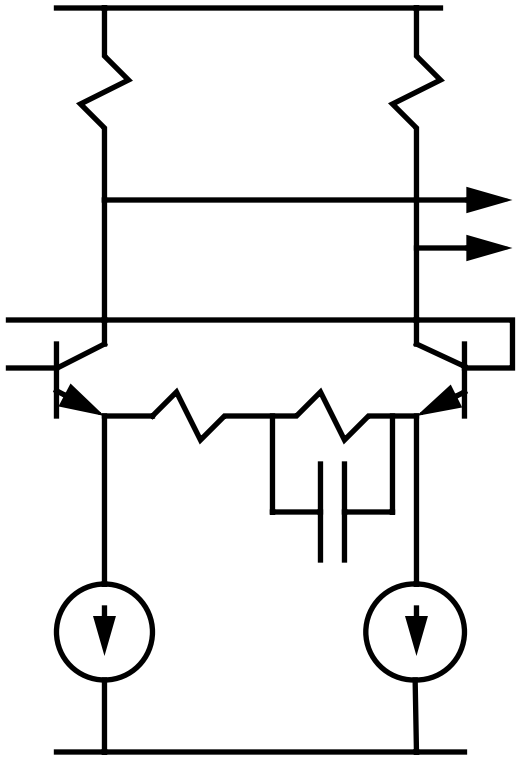
before



after

Skin Loss Equalization at Receiver





[WWS92]

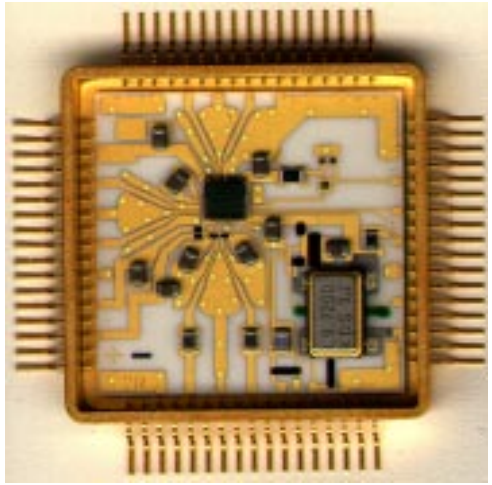
Agenda

- Overview of Serial Data Communications
- Signal Degradation Mechanisms
- Data Coding Techniques
- Clock Recovery Methods
- Components Used in Clock/Data Recovery
- Jitter Measurements

Diversity of CDR applications

- Clock and Data Recovery (CDR) applications span the range from ultra-high-volume, low cost datacom applications to very high precision, long-haul telecom applications
- Many different trade-offs are made to tailor each circuit to the target application area

1.25Gb/s Gigabit Ethernet Transceiver <$10 in volume (datacom application)

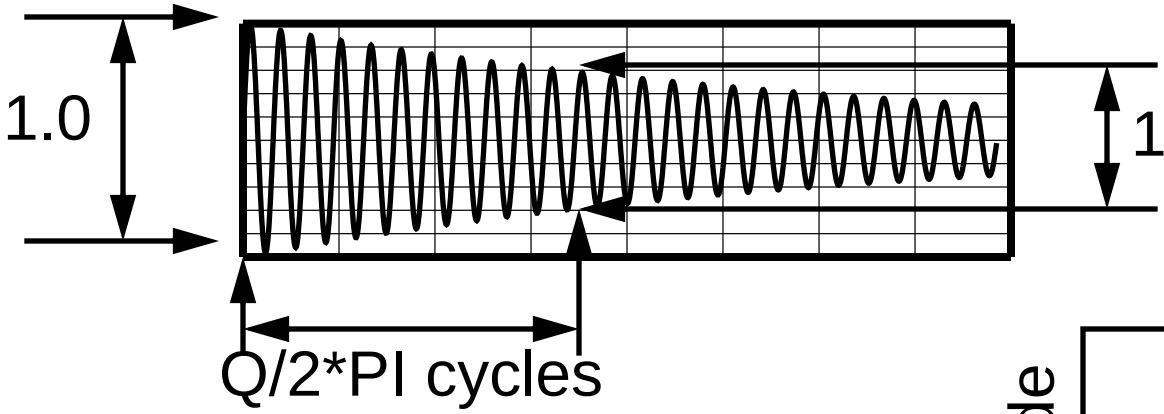


1cm

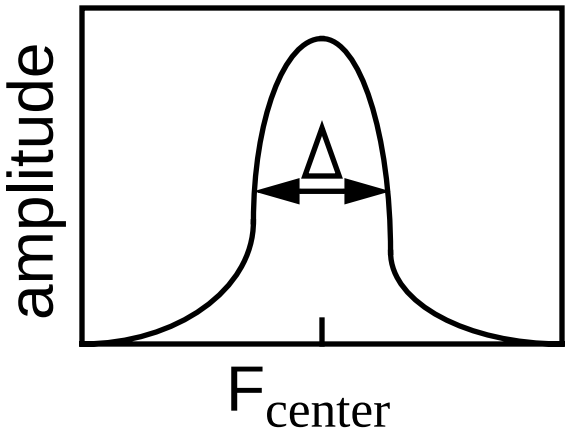
2.488Gb/s SONET CDR ~$500 (telecom application)

Q-Factor in resonant circuits

Voltage envelope of ringing circuit falls to 1/sqrt(e) in Q radians.



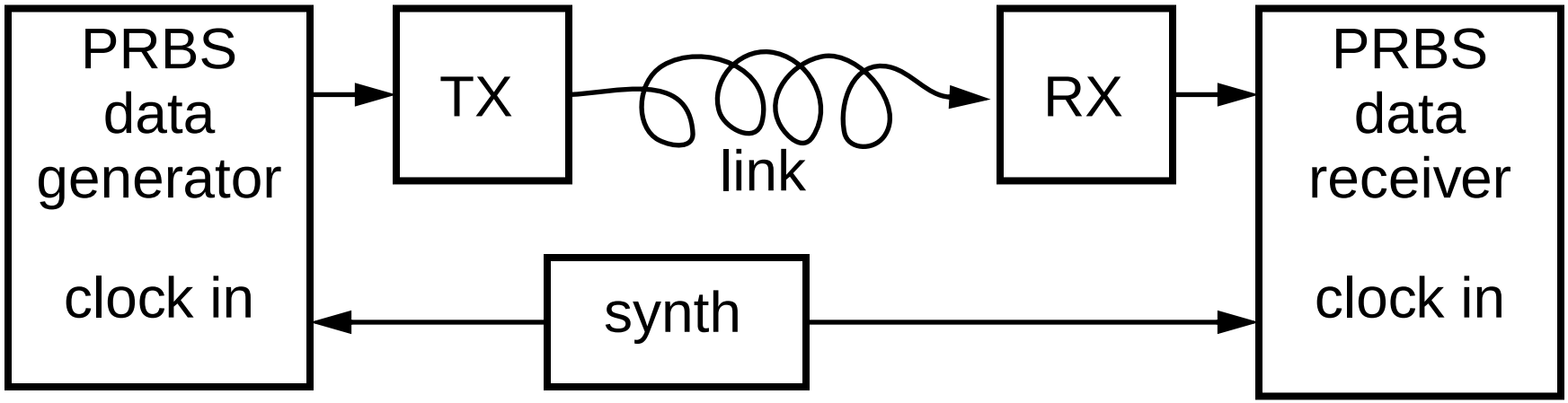
Q also equals the center frequency of a filter divided by the full-width of the resonance measured at the half power points: F_{center}/Δ



High-Q filter can be emulated by PLL with low loop B.W.

Bit Error Rate (BER) Testing

- Pseudo-Random-Bit-Sequence (PRBS) is used to simulate random data for transmission across the link
- PRBS pattern 2^N-1 Bits long contains *all* N-bit patterns
- Number of errored-bits divided by total bits = BER.
- Typical links are designed for BERs better than 10^{-12}

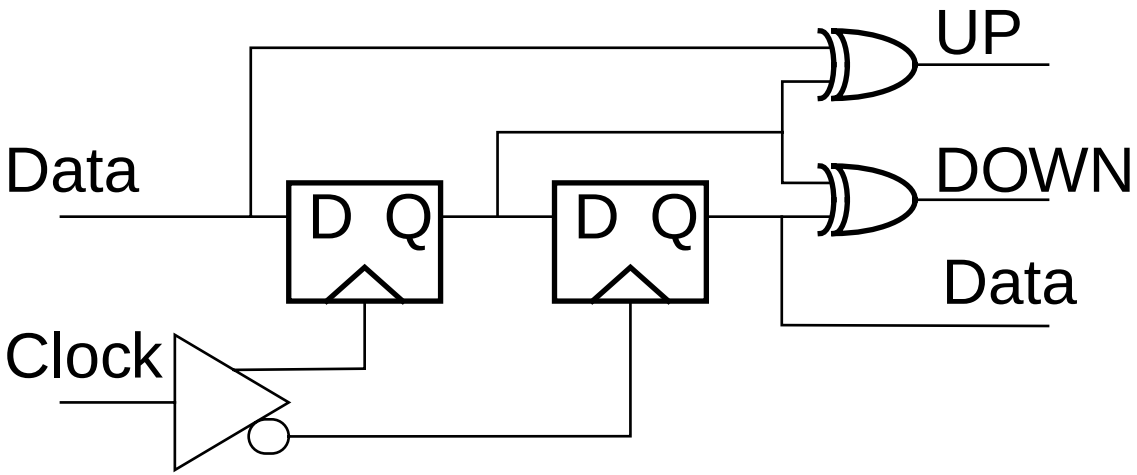


Drawbacks of Simple PLL

1) timing pulses
2) transfer function (linear vs BB),
3) quadratic, BB
4) critical problem is the stuttering data

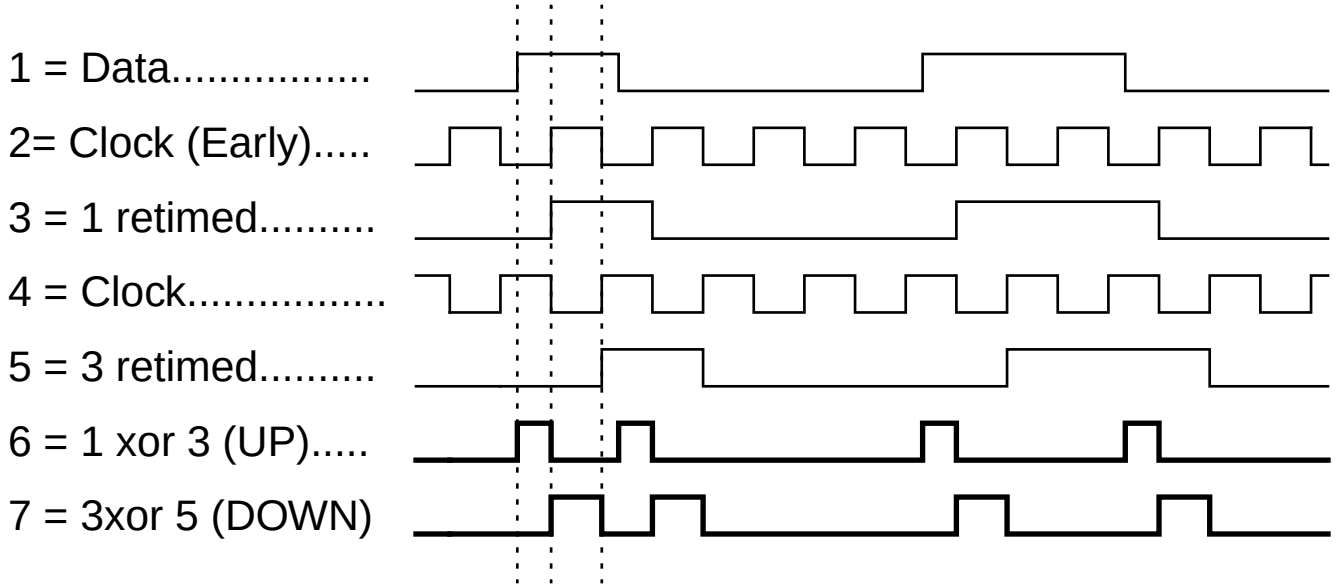
??

“Self-Correcting Phase Detector”



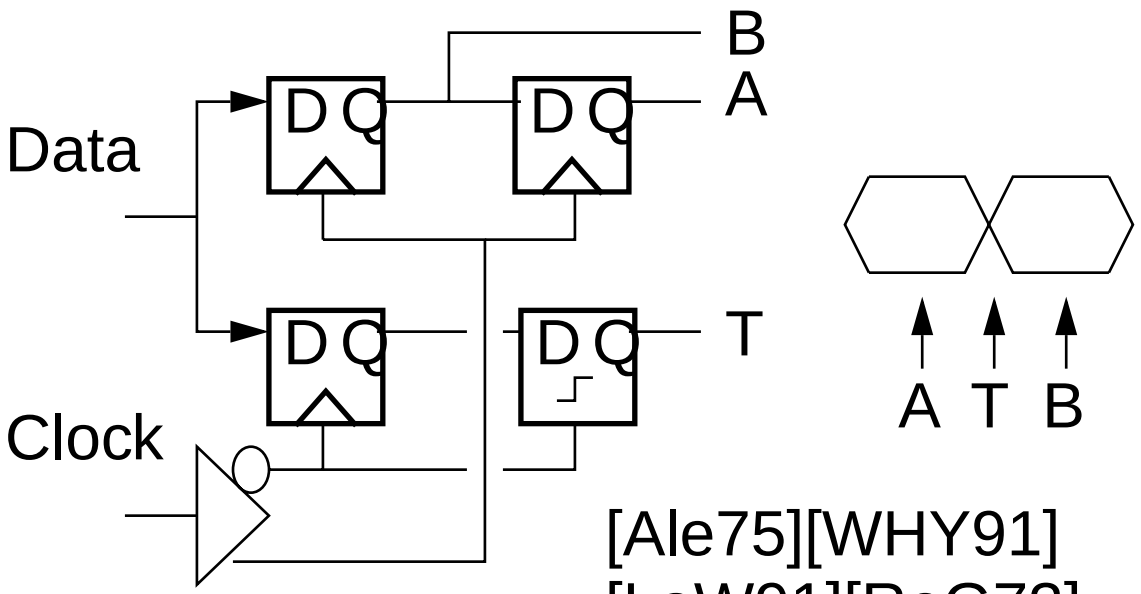
See FA9.6, 1997 ISSCC

[Hog85][Shi87]



Binary Quantized Phase Detector

- NRZ data is sampled at each bit cell and near the transitions of each bit cell
- The sign of the transition sample is compared with the preceeding and following bit cell sample to deduce the phase error



[Ale75][WHY91]
[LaW91][ReG73]

A	T	B	Output
0	0	0	tristate
0	0	1	vco fast
0	1	0	?
0	1	1	vco slow
1	0	0	vco slow
1	0	1	?
1	1	0	vco fast
1	1	1	tristate

CDR Design Checklist

1) Eye Margin

- how much noise can be added to the input signal while maintaining target BER? (voltage margin)
- How far can clock phase alignment be varied while maintaining target BER? phase margin)
- how much does the static phase error vary versus frequency, temperature and process variation?
- Is input amplifier gain, noise and offset sufficient?

CDR Design Checklist (cont)

2) Jitter Characteristics

- what is the jitter generation? (VCO phase noise, etc)
- what is the jitter transfer function? (peaking and bandwidth)what is the jitter tracking tolerance versus frequency?

CDR Design Checklist (cont)

3) Pattern Dependency

- how do long runlengths affect system performance?
- is bandwidth sufficient for individual isolated bit pulses?
- are there other problematic data patterns? (resonances)
- does PLL bandwidth, jitter, and stability change versus transition density?

4) Acquisition Time

- what is the initial, power-on lock time?
- what is the phase-lock aquisition time when input source is changed?

CDR Design Checklist (cont)

5) How is precision achieved?

- are external capacitors, inductors needed?
- does the CDR need an external reference frequency?
- are laser-trimming or highly precise IC processes required?

6) Input/output impedance

- Is S11/S22 (input/output impedance) maintained across the frequency band?
- are reflection large enough to lead to eye closure and pattern dependency?
- is t >15 dB return loss maintained across the band?

CDR Design Checklist (cont)

7) Power Supply

- does the CDR create power supply noise?
- how sensitive is the CDR to supply noise?
- Is the VCO self-modulated through its own supply noise? (can be “deadly”)
- what is the total static power dissipation?
- what is the die temperature under worse case conditions?

CDR Design Checklist (cont)

8) False lock susceptibility

- can false lock occur?
- are false lock conditions be detected and eliminated?
- can the VCO run faster than the phase/frequency detector can operate? (another “killer”)
- have all latchup/deadly embrace conditions been considered and eliminated?