Clock and Data Recovery for Serial Digital Communication

(plus a tutorial on bang-bang Phase-Locked-Loops)

Rick Walker

Hewlett-Packard Company

Palo Alto, California

walker@opus.hpl.hp.com

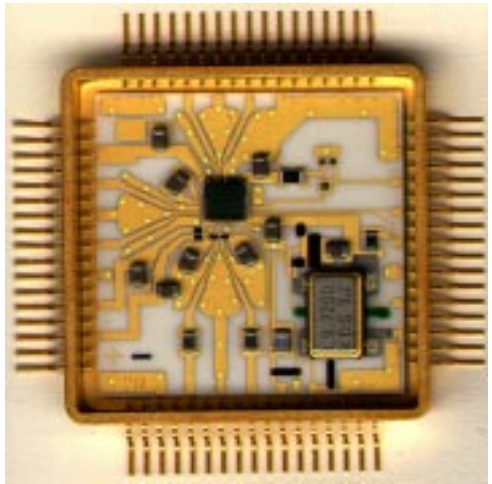
Agenda

- Overview of serial data communications
  - Degradation mechanisms, data coding
  - Clock recovery methods and components
  - Jitter measurements
- *Break*
- BB PLL Theory
  - Simulation techniques
  - 1st, 2nd order loops
  - Key design parameters

Diversity of CDR applications

- Clock and Data Recovery (CDR) applications span the range from ultra-high-volume, low cost datacom applications to very high precision, long-haul telecom applications
- Many different trade-offs tailor each circuit to the target application area

1.25Gb/s Gigabit Ethernet Transceiver <$6 in volume (datacom application)



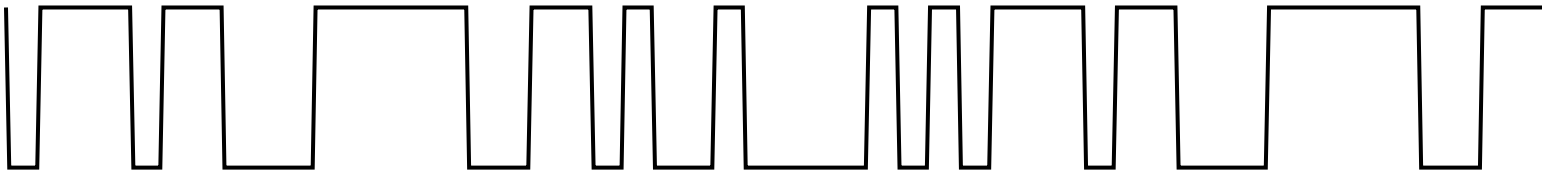
1cm

2.488Gb/s SONET CDR ~$400 (telecom application)

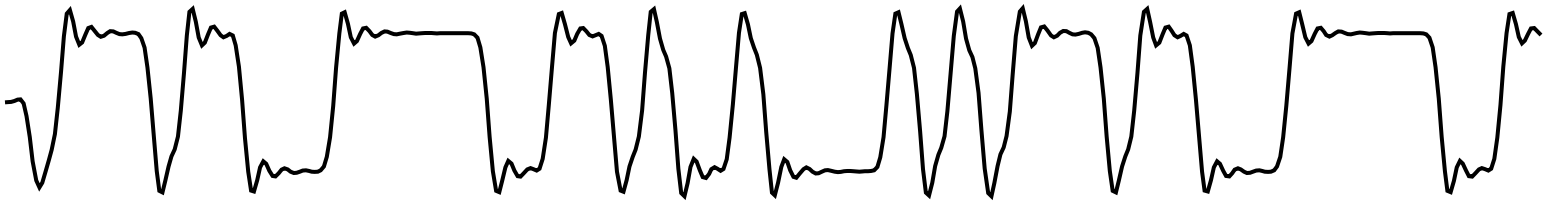
Basic Idea

Serial data transmission sends binary bits of information as a series of optical or electrical pulses:

01110110001111100110100100001010111011000111111..



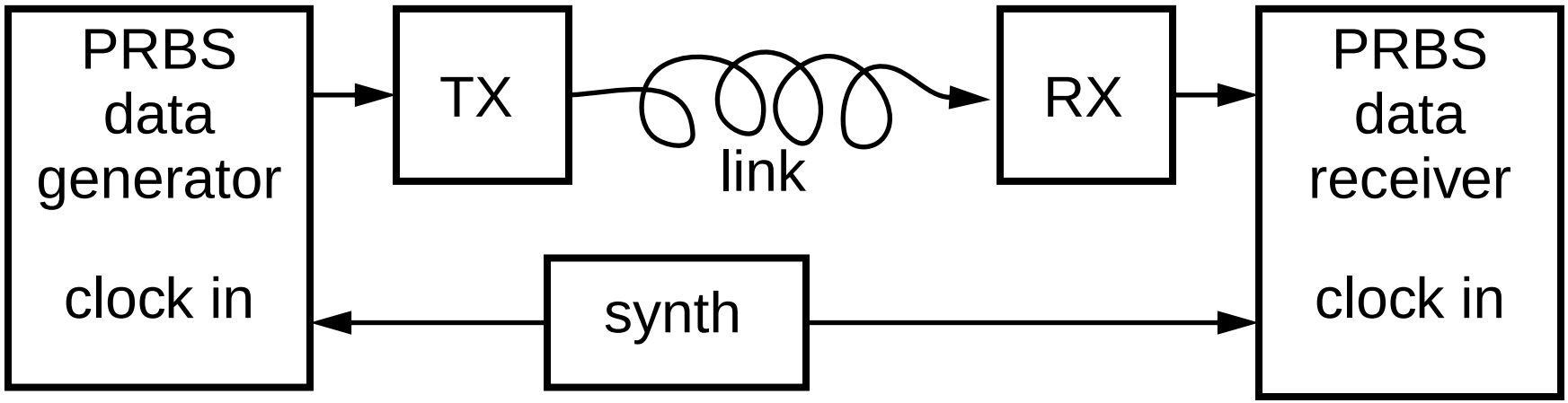
The transmission channel (coax, radio, fiber) generally distorts the signal in various ways:



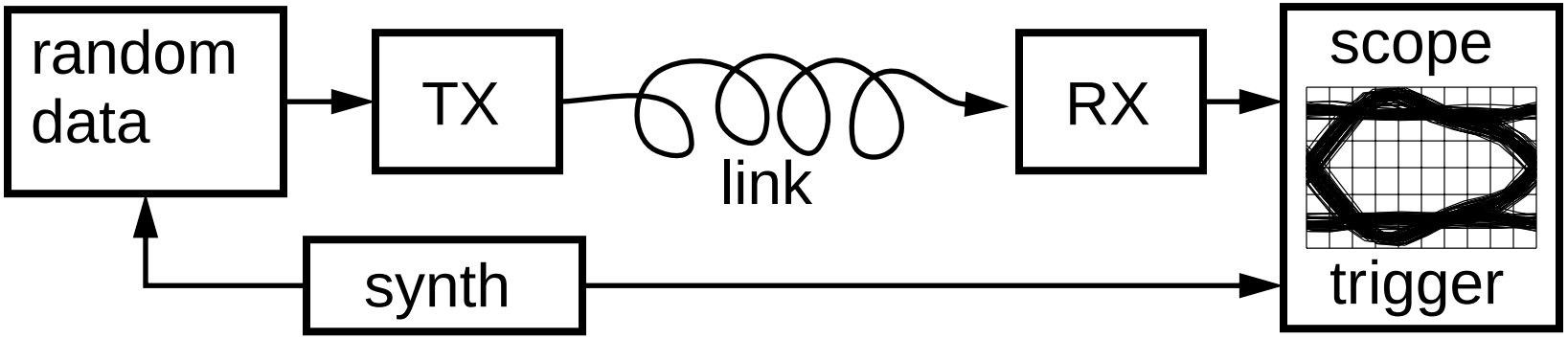
From this signal we must recover both clock and data

Bit Error Rate (BER) Testing

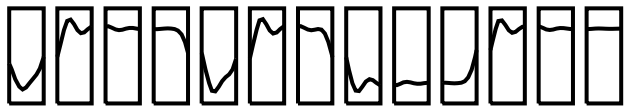
- Pseudo-Random-Bit-Sequence (PRBS) is used to simulate random data for transmission across the link
- PRBS pattern 2^N-1 Bits long contains *all* N-bit patterns
- Number of errored-bits divided by total bits = BER.
- Typical links are designed for BERs better than 10^{-12}



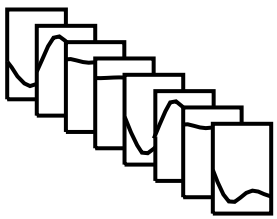
Eye diagram construction

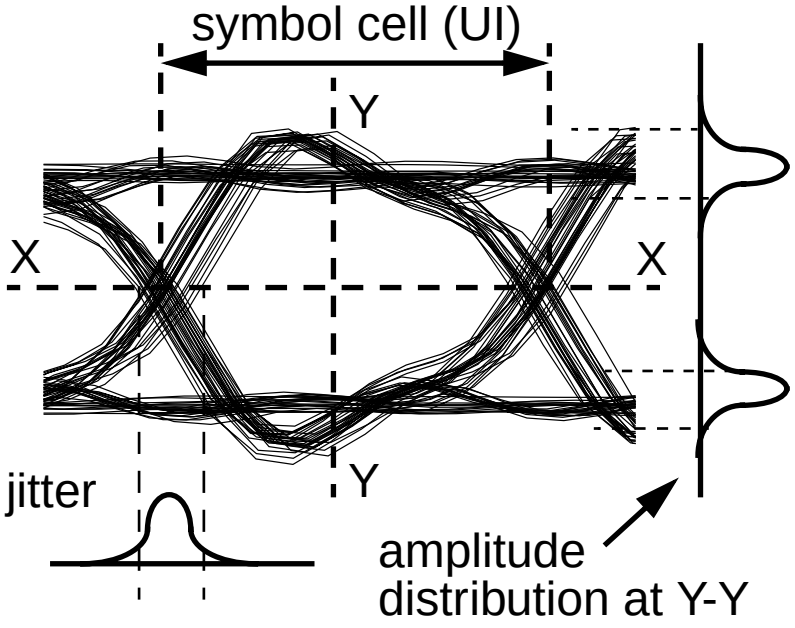


Use a precise clock to chop the data into equal periods



overlay each period onto one plot

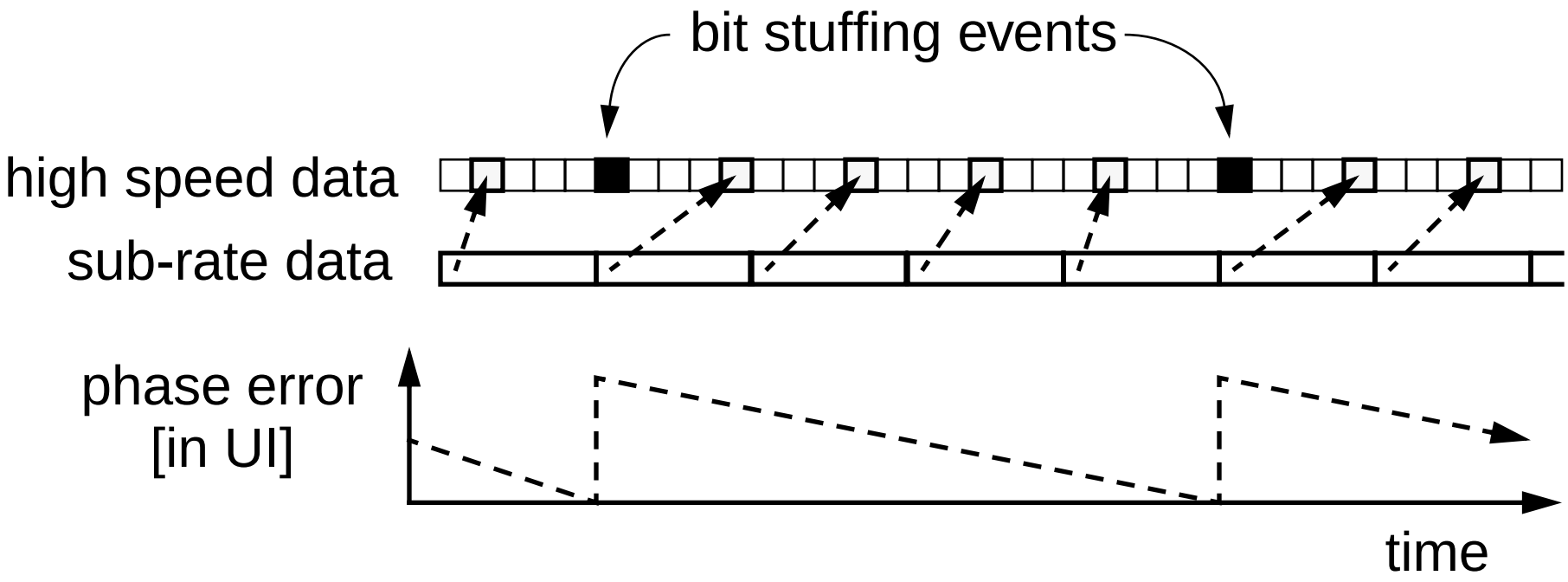




Some Signal Degradation Mechanisms

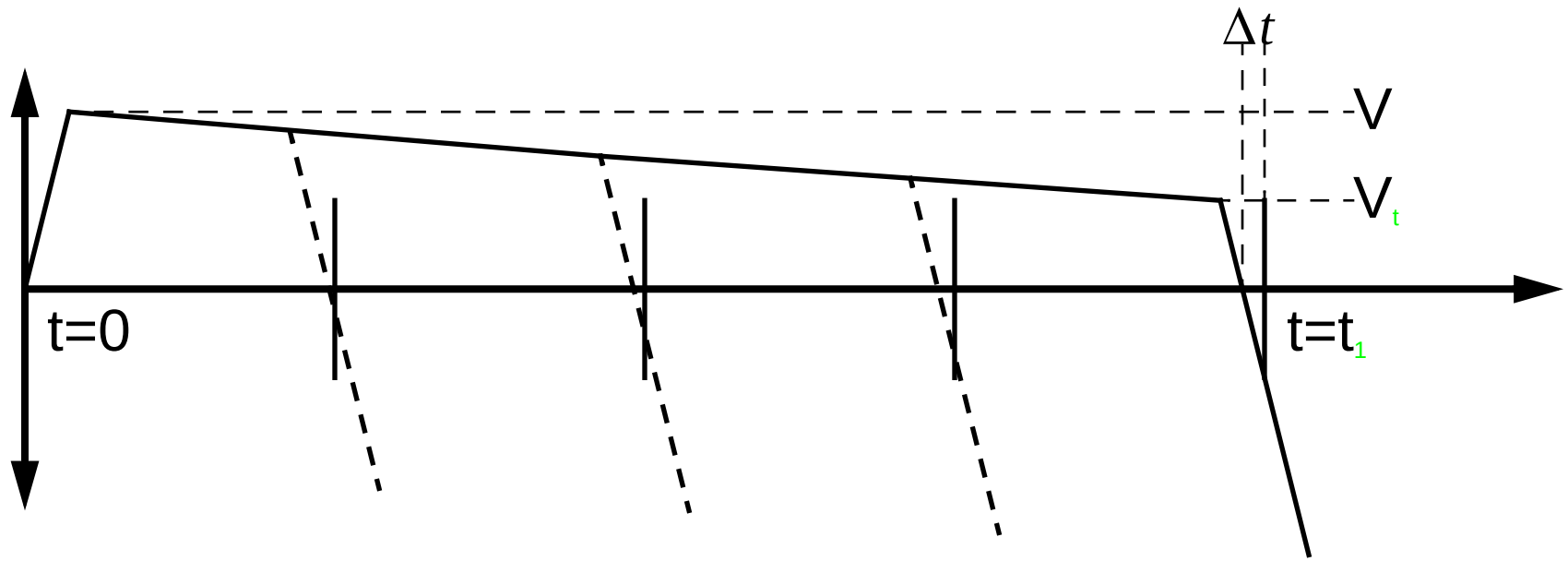
- Multiplex Jitter
- AC Coupling
- Optical Pulse Dispersion
- Skin Loss
- Random Noise
- E+O Crosstalk
- Intersymbol Interference

Multiplex Jitter



Multiplex jitter is not a problem on the high rate channel itself - it only occurs on non-synchronous, lower speed tributaries that have been sent over the high-speed channel (e.g.: DS3 over SONET OC-48).

Time/Voltage aberrations from AC-coupling

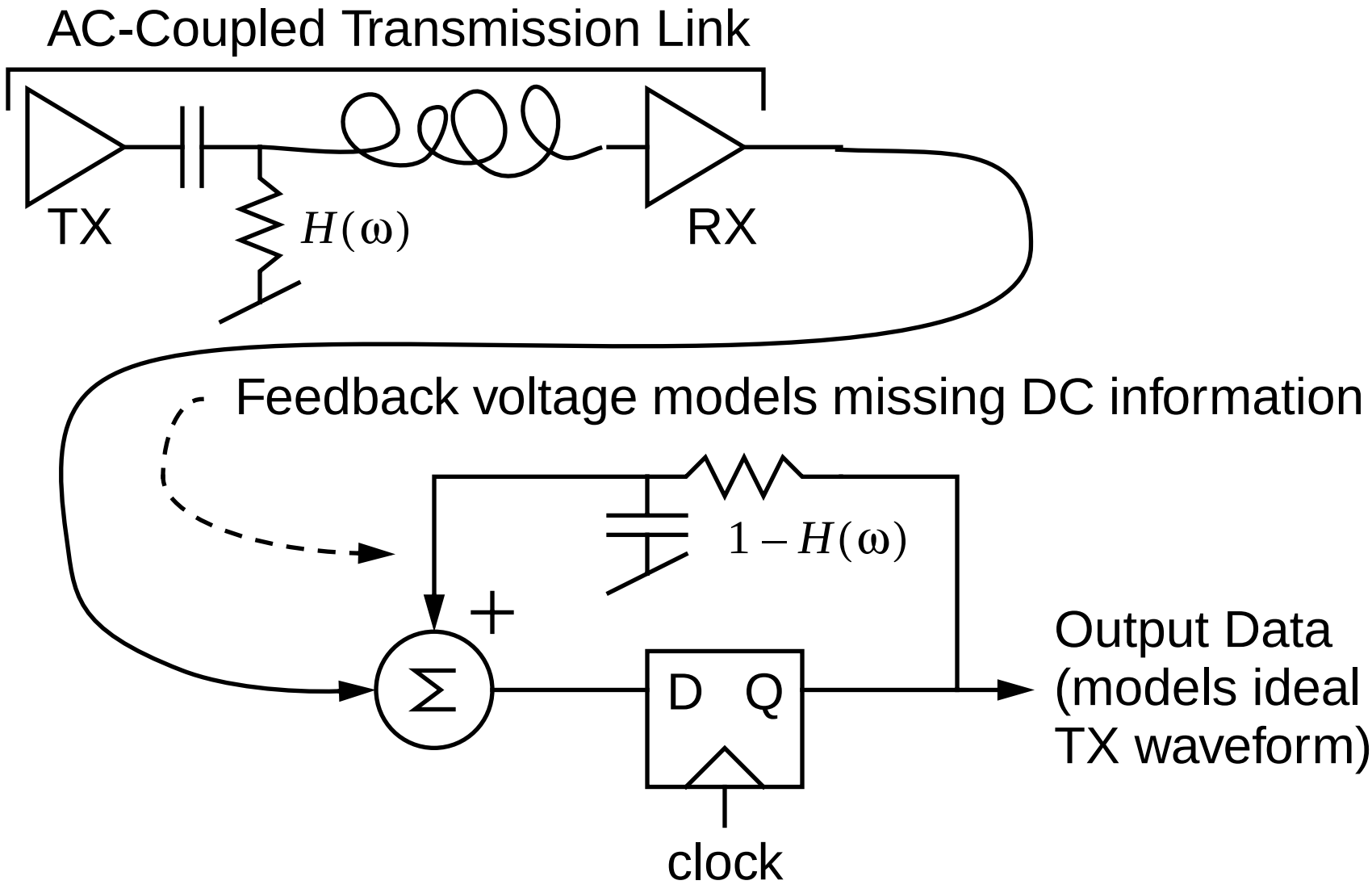


Percent AC coupled droop is $P \equiv \frac{V - V_t}{V} \times 100 \approx \frac{t_1}{RC} \times 100$.

Jitter is introduced by finite slope of pulse rise/fall time:

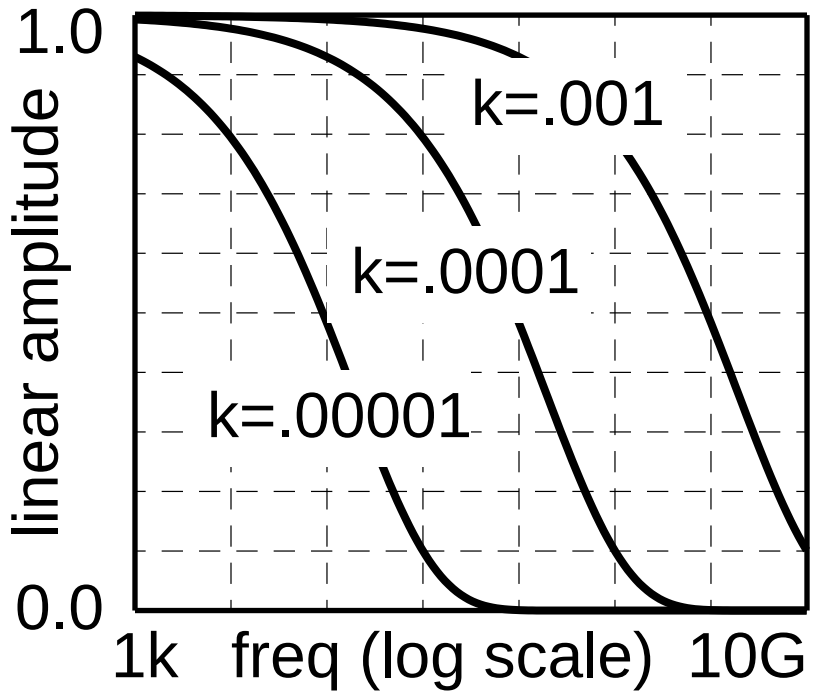
$$\Delta t = \frac{t_r t_1}{(2RC)}$$

Quantized Feedback

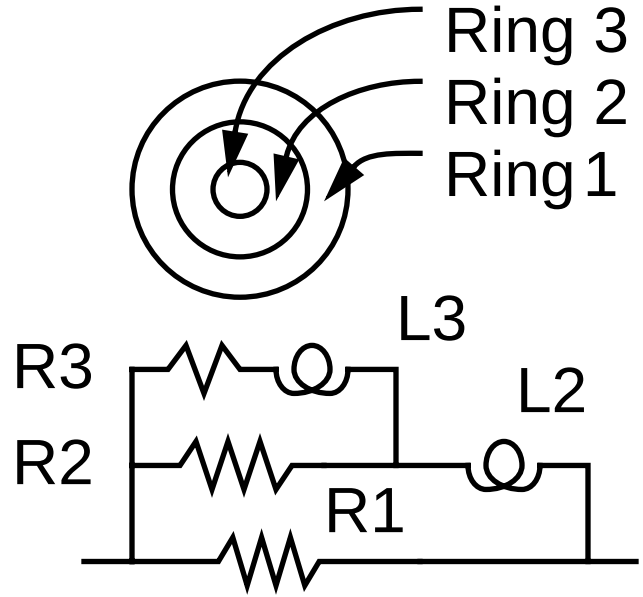


Skin Loss and Dielectric Loss

Nearly all cables are well modelled by a product of Skin Loss $S(f) = 10^{(-k)\sqrt{f}}$, and Dielectric Loss $D(f) = 10^{(-l)f}$ with appropriate k,l factors. Dielectric Loss dominates in the multi-GHz range. Both plot as straight lines on log(dB) vs log(f) graph.

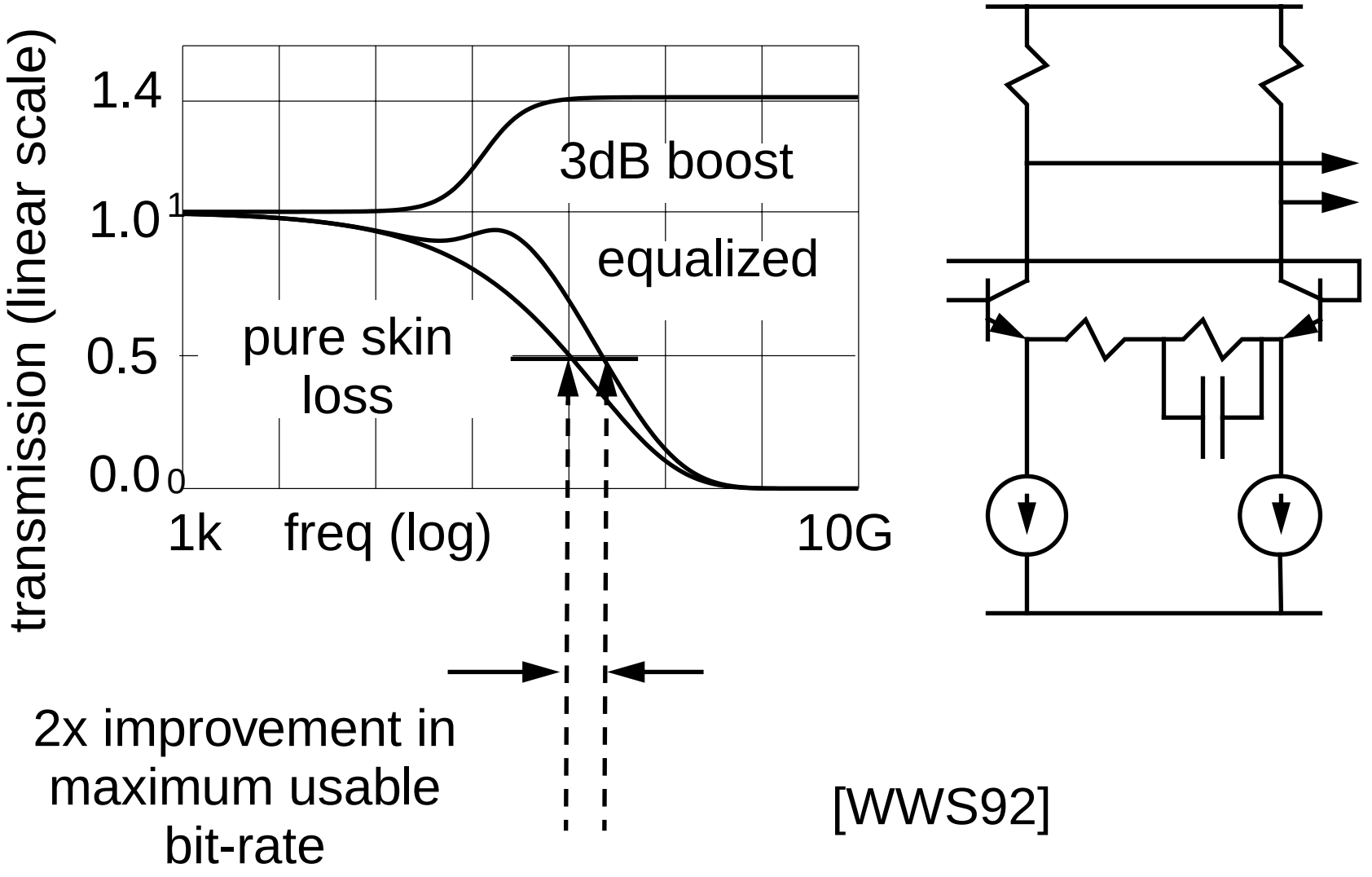


[YFW82]



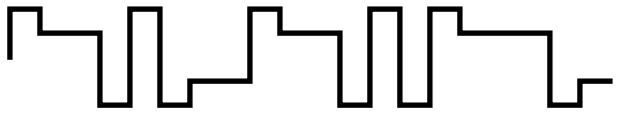
Three-element equivalent circuit of a conductor with skin loss

Skin Loss Equalization at Receiver

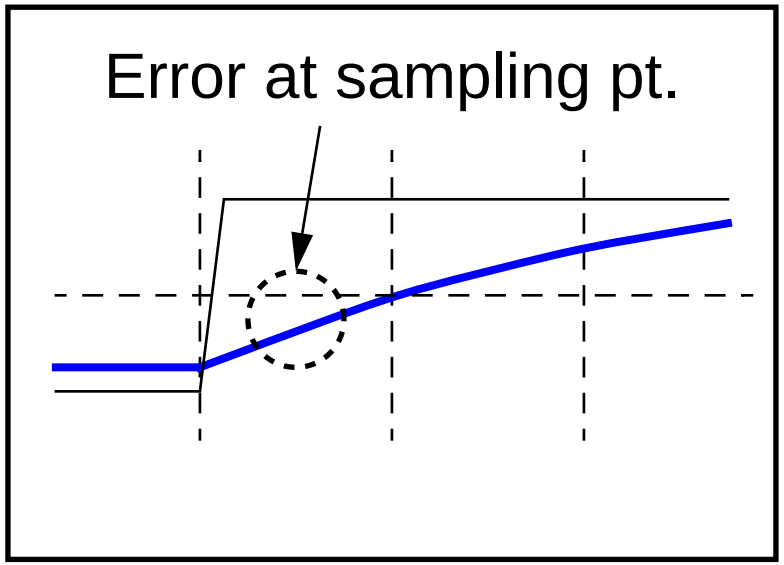


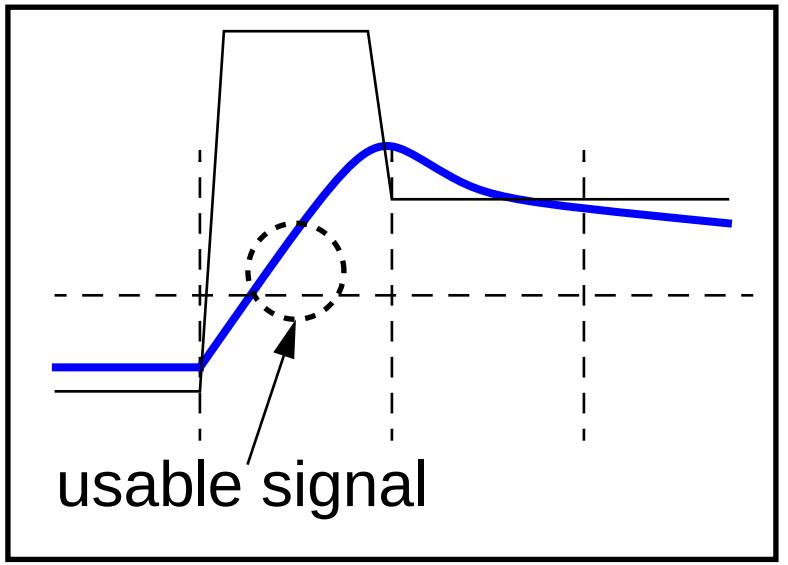
[WWS92]

Skin Loss Equalization at Transmitter

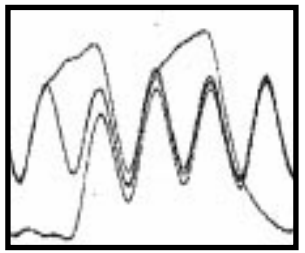


boost the first pulse after every transition

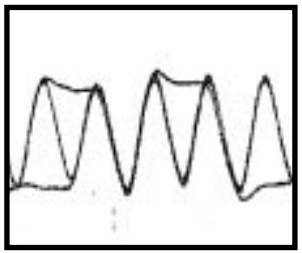




[FMW97]



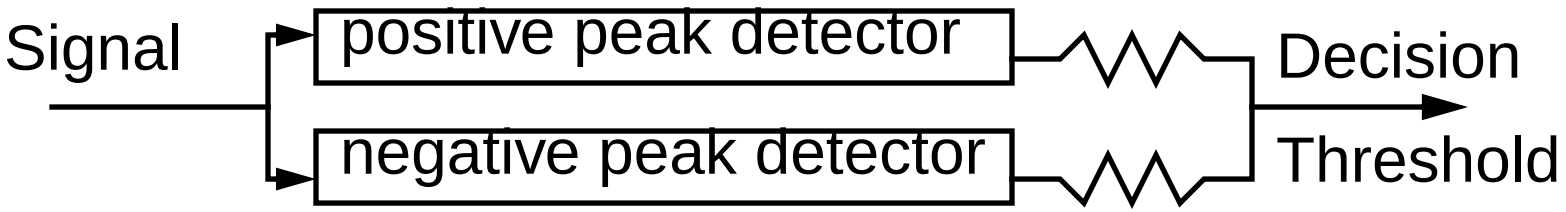
before



after

Decision Threshold Generation

- To minimize bit-error rate, the decision threshold X-X must centered in the signal swing. Two common ways of automatically generating threshold voltage are:
  - Peak detection of signal extremes, limited run-length required

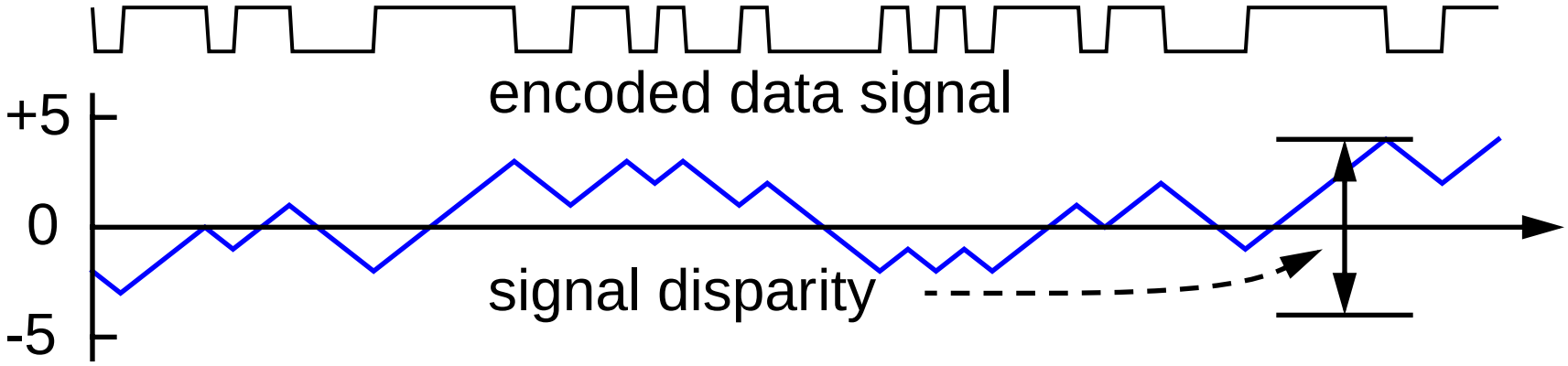


  - Decision threshold = signal average, balanced signal required

After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

Code Disparity

Disparity is defined as $N_{high} - N_{low}$ in past transmitted signal



- In an *unbalanced* code the disparity can grow without limit. e.g.: 4B5B code of FDDI
- In a *balanced* code, the disparity is limited to a finite worst case value. e.g.: 8B10B of FibreChannel

After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

Coding for Desirable Properties

- DC balance, low disparity
- Bounded run length
- High Coding Efficiency
- Spectral Properties (decrease HF and/or DC component)
- *Many Variations are Possible!*
  - Manchester [San82]
  - mB/nB [Gri69][Rou76][WiF83] [YKI84] [Pet88]
  - Scrambling [CCI90]
  - CIMT [WHY91], Conservative Code [Ofe89]

Simple 3B/4B code example

3B Input Data	4B Output Data	
	Even Words	Odd Words
000	0011	
001	0101	
010	0110	
011	1001	
100	1010	
101	1100	
110	0100	1011
111	0010	1101
SyncA	0111	1110
SyncB	1000	0001

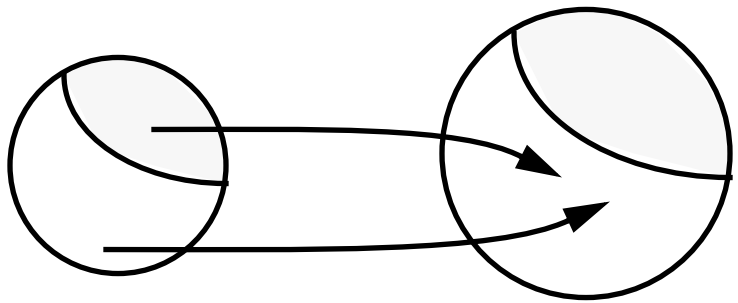
Maximum Runlength is 6

Coding Efficiency is 4/3

Sending Sync Sequence:

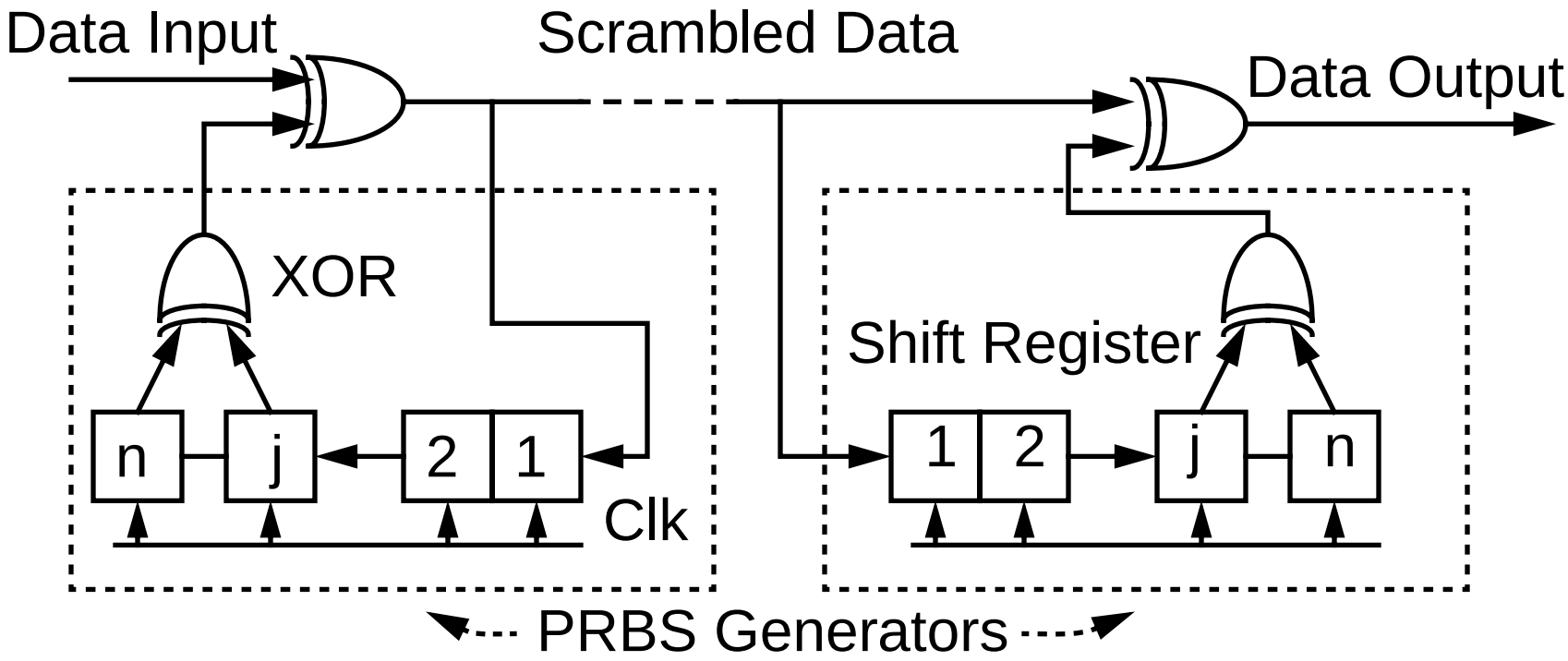
SyncA(even), SyncA(odd), SyncB(even), SyncB(odd)

allows the unambiguous alignment of 4-bit frame

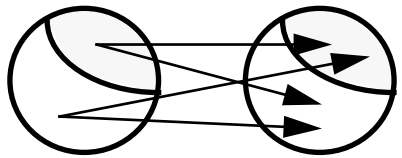


Scrambling

- Uses a feedback shift register to randomize data - reversing process at receiver restores original data

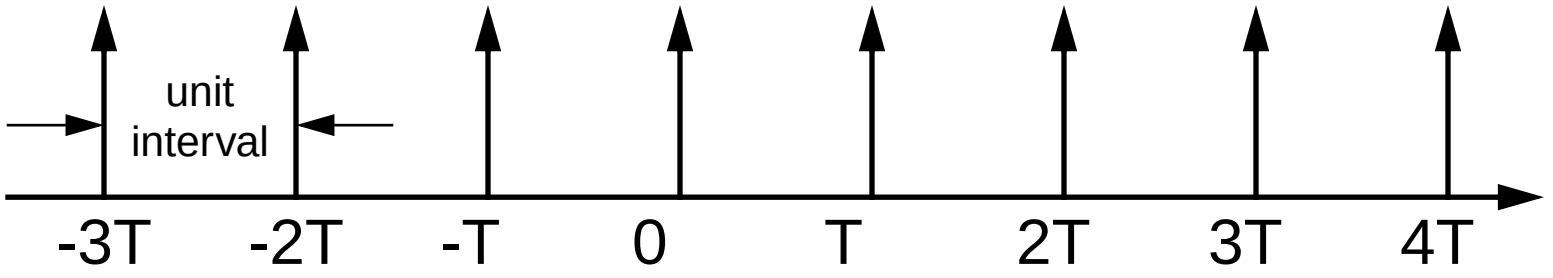


Caveat: Only guarantees balance and run-length under very specific data conditions!

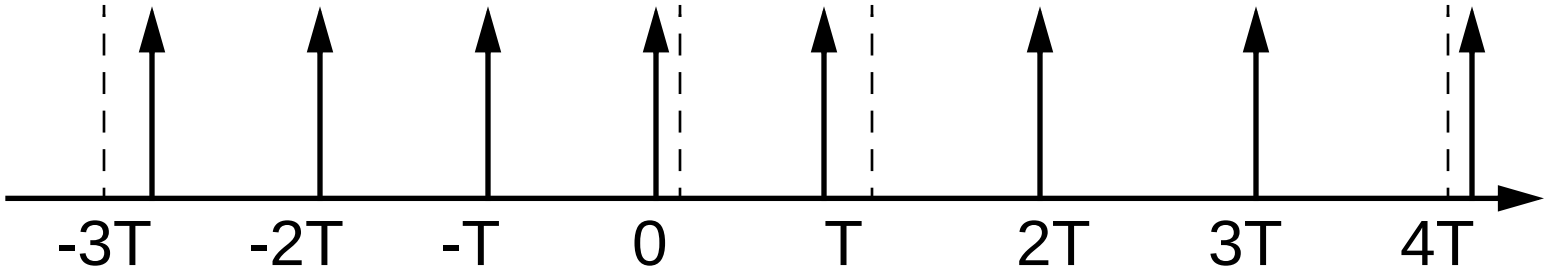


After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

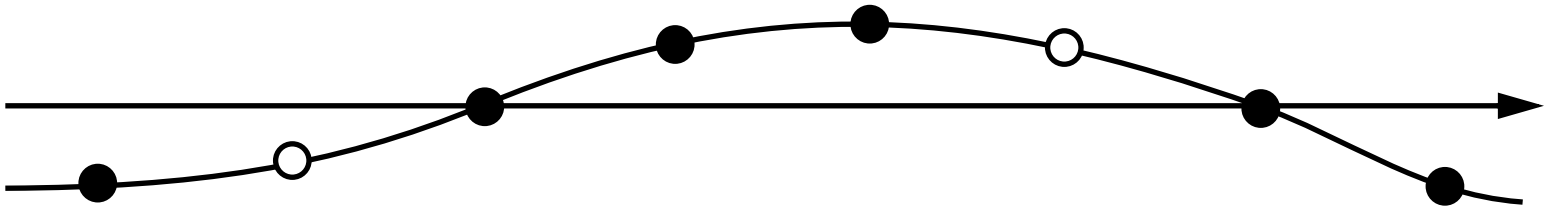
Definition of Jitter



Impulses spaced equally in time (jitter free signal)



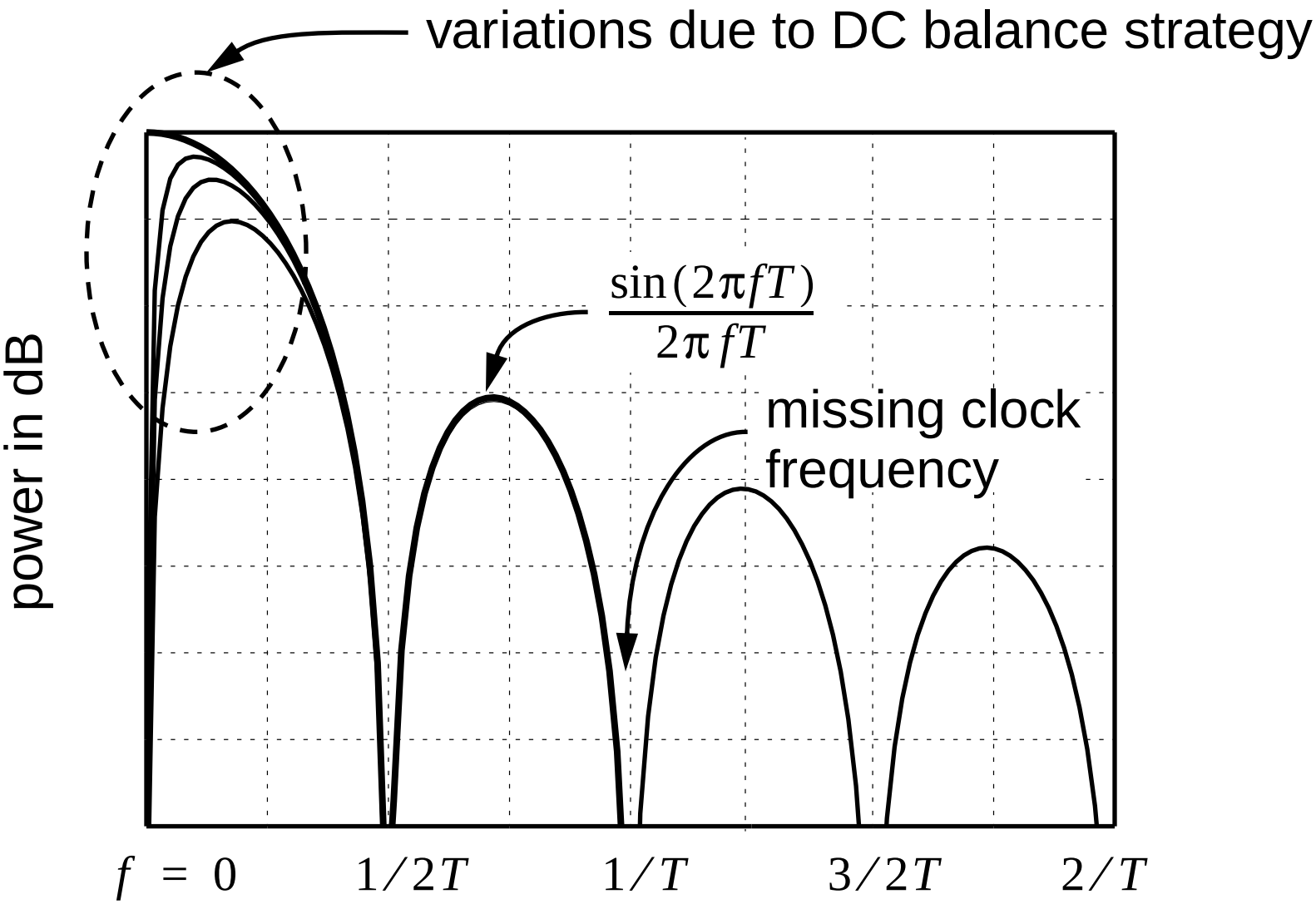
Impulses spaced irregularly in time (jittered signal)



Errors treated as discrete samples of continuous time jitter

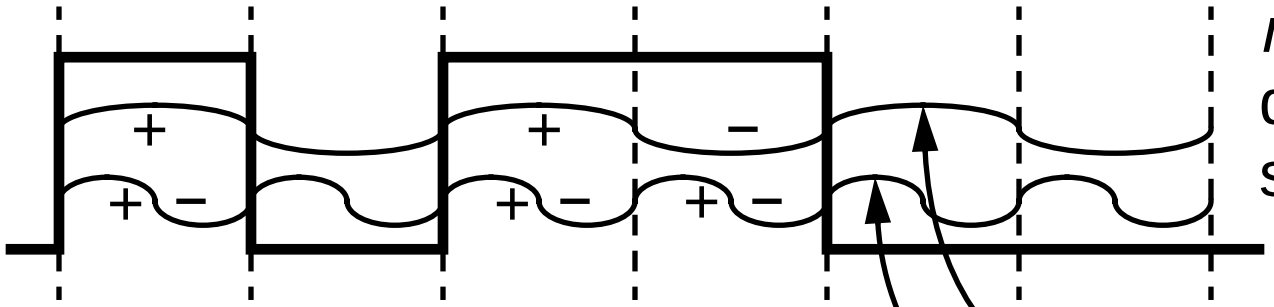
After Trischitta and Varma: “Jitter in Digital Transmission Systems”

Spectrum of NRZ data



NRZ and RZ signalling

NRZ = “non return to zero” data

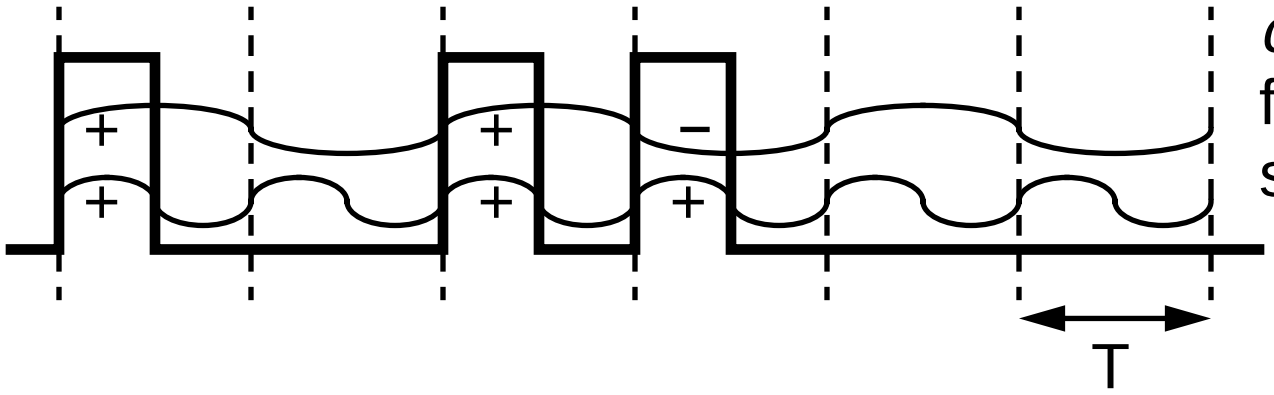


neither clock *nor* data frequency in spectrum

data frequency

clock frequency

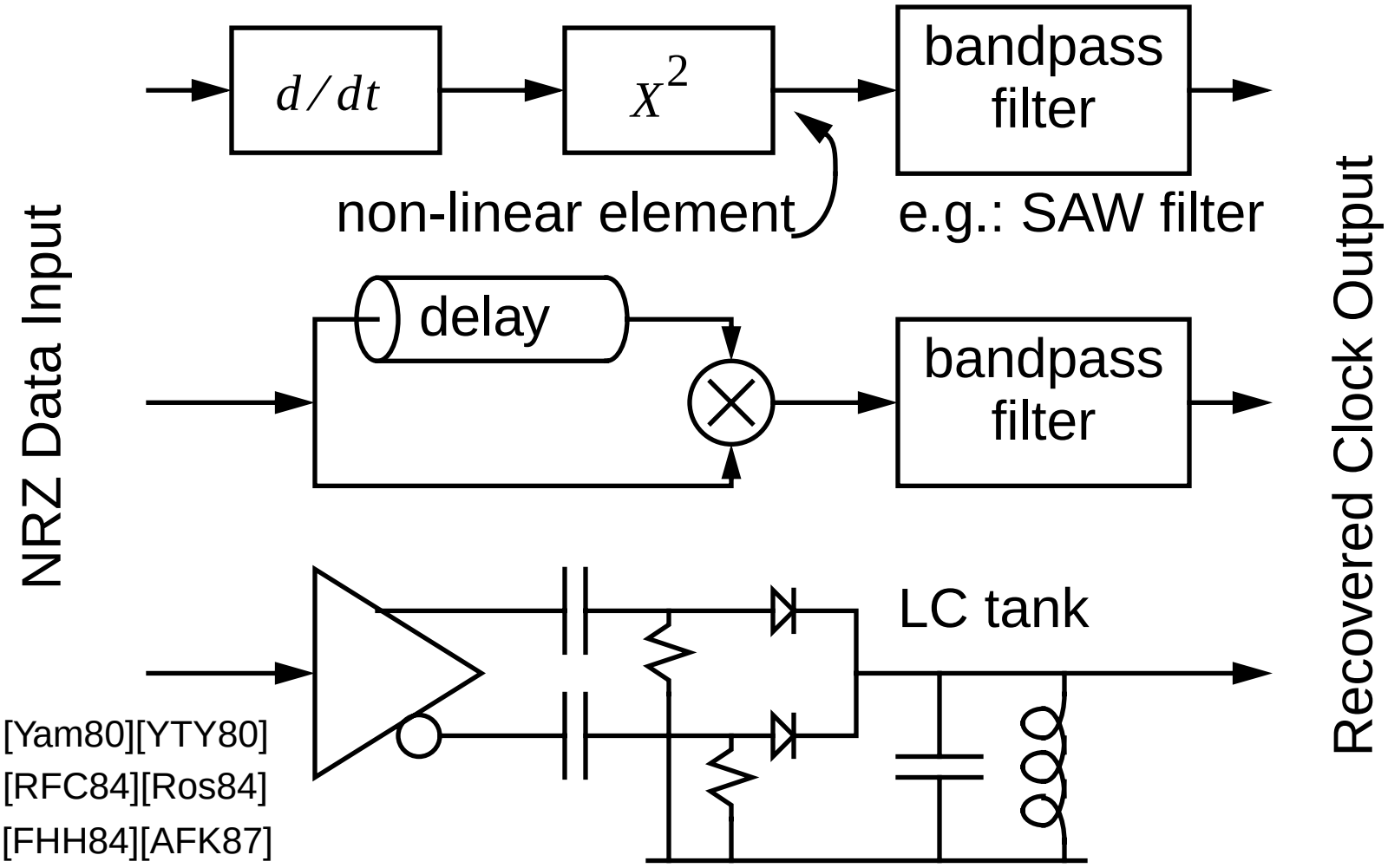
RZ = “return to zero” data



clock, but *no* data frequency in spectrum

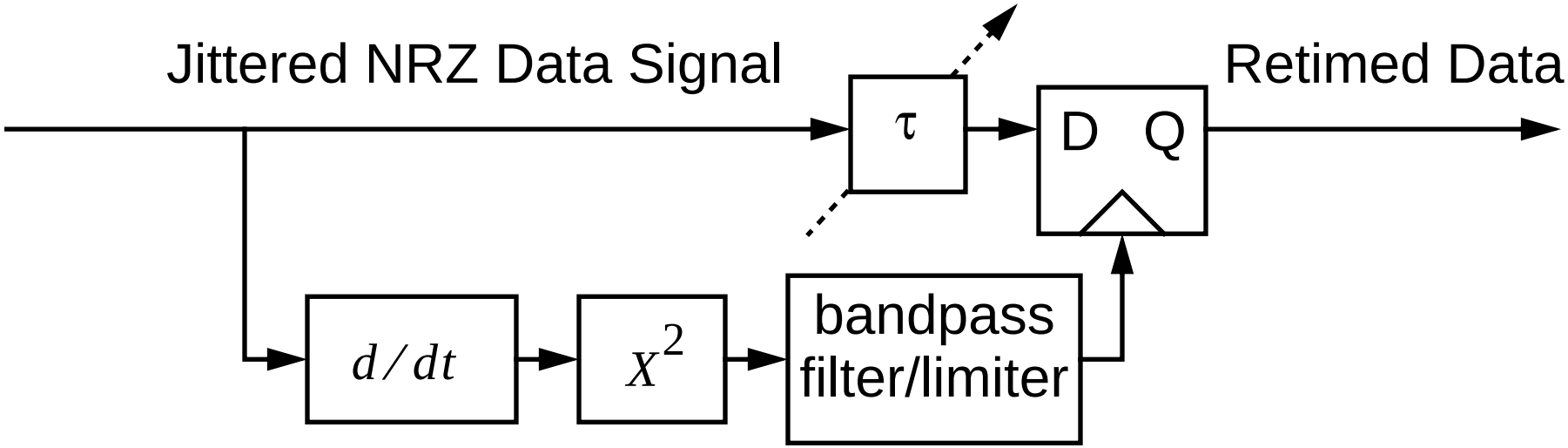
NRZ signalling is almost universally used.

Filter Method Examples



(this last circuit can be thought of as an NRZ-RZ converter)

Summary of Filter Method



Pro:

Very simple to implement

Can be built with microwave “tinkertoys” using coax to very high frequencies

Con:

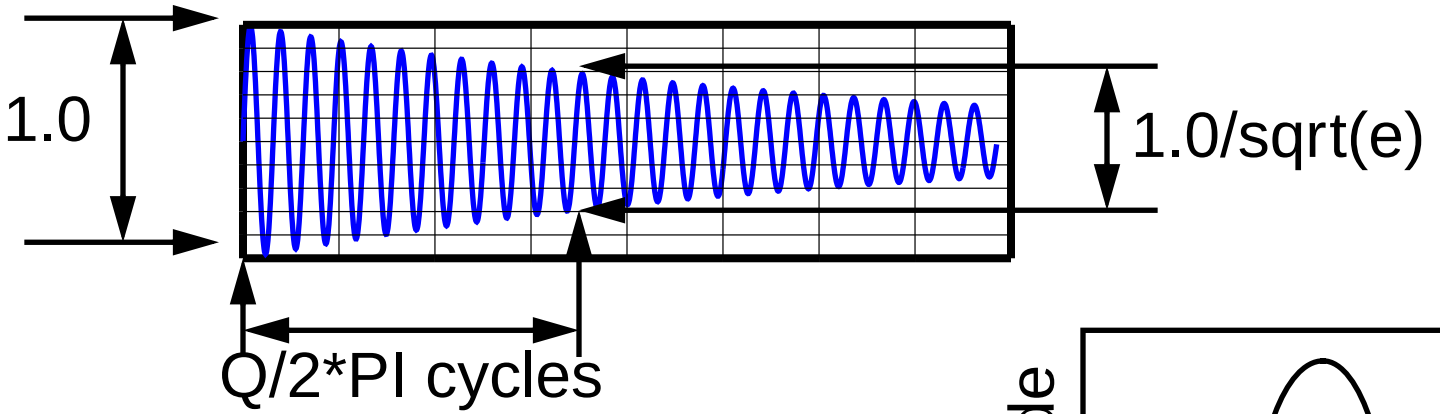
Temperature and frequency variation of filter group delay makes sampling time difficult to control

Narrow pulses imply high f_T

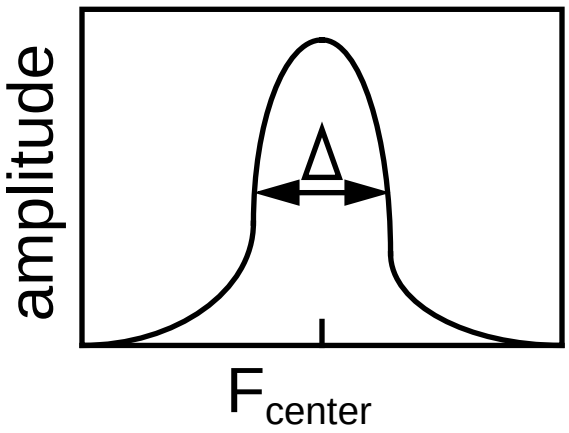
Hi-Q filter difficult to integrate

Q-Factor in resonant circuits

Voltage envelope of ringing circuit falls to 1/sqrt(e) in Q radians.

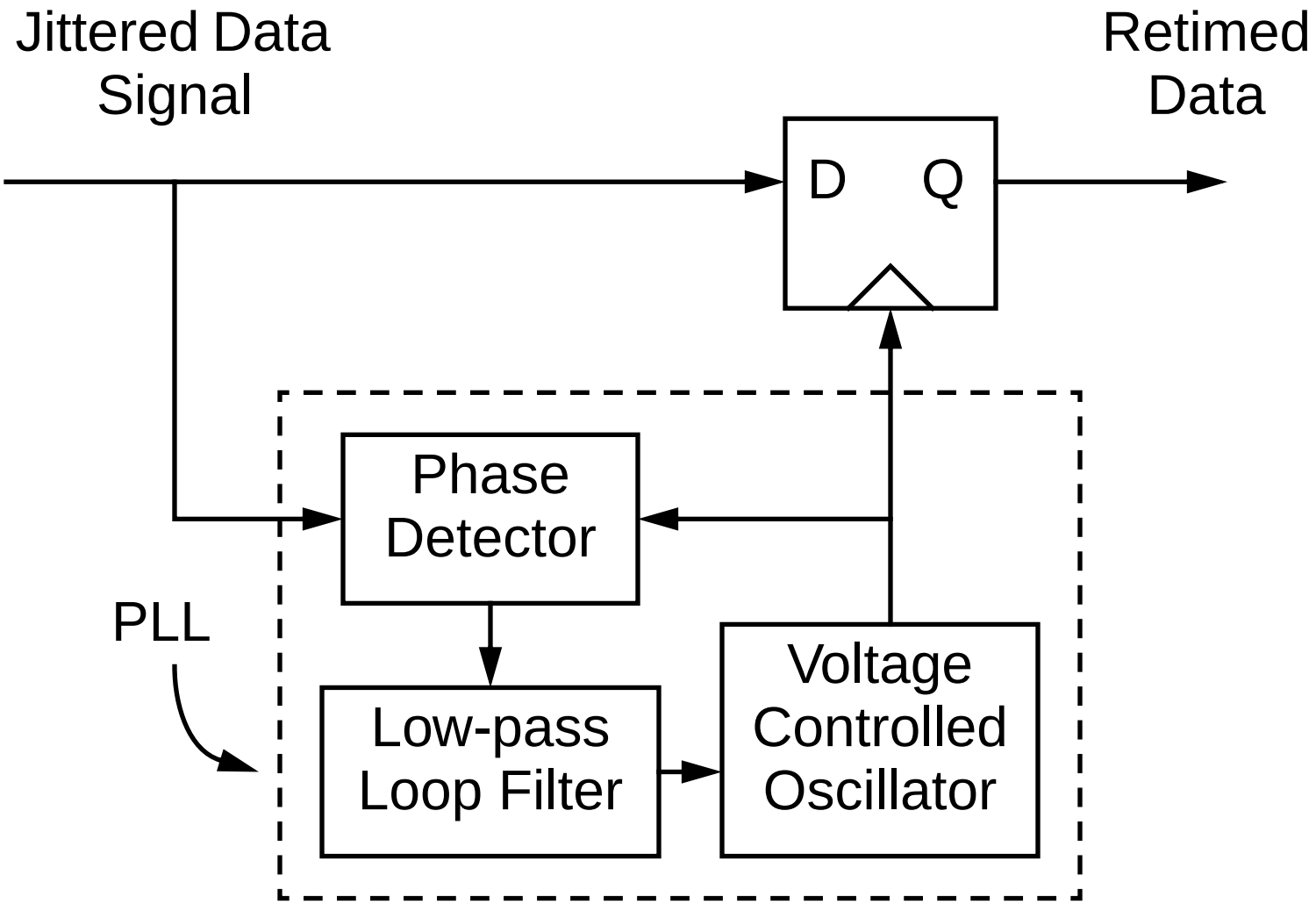


Q also equals the center frequency of a filter divided by the full-width of the resonance measured at the half power points: $F_{center}/\ \Delta$

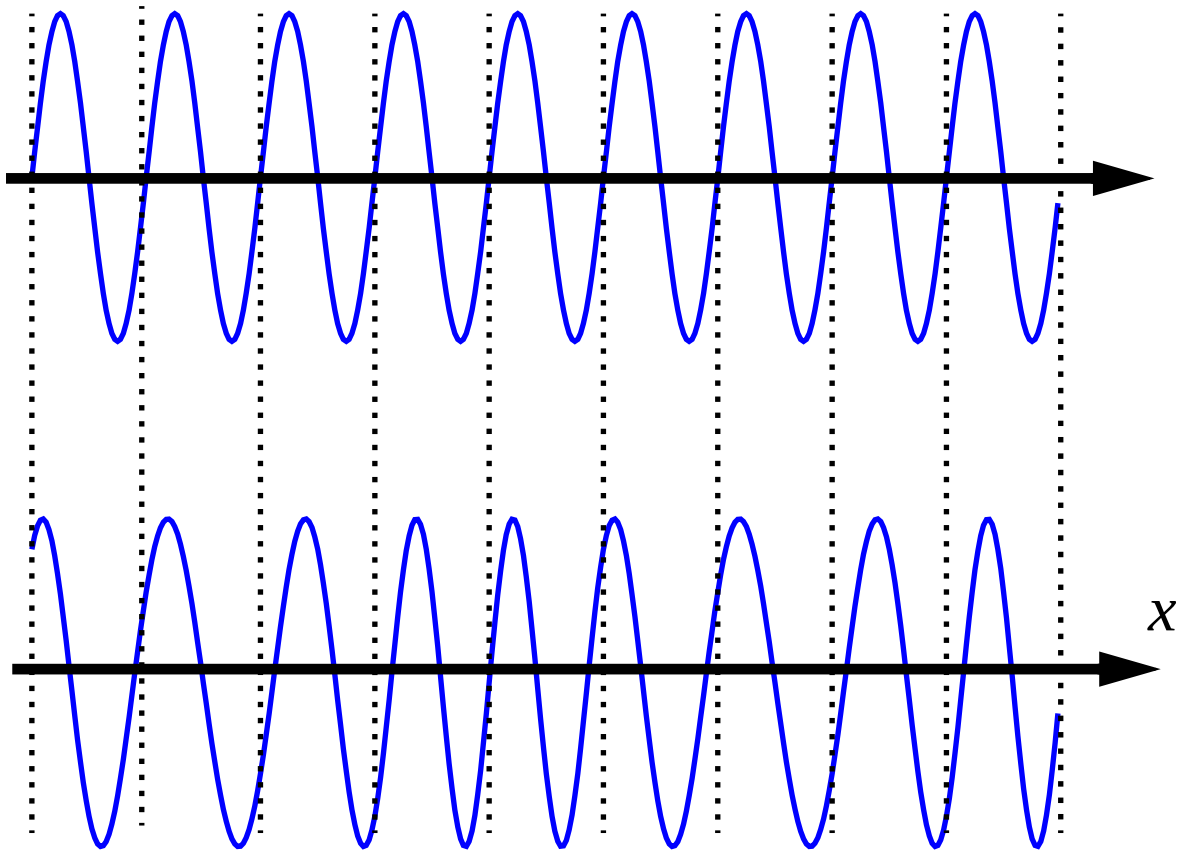


High-Q filter can be emulated by PLL with low loop B.W.

Data Recovery with simple PLL



Analytic Treatment of Jitter



Perfect Clock:

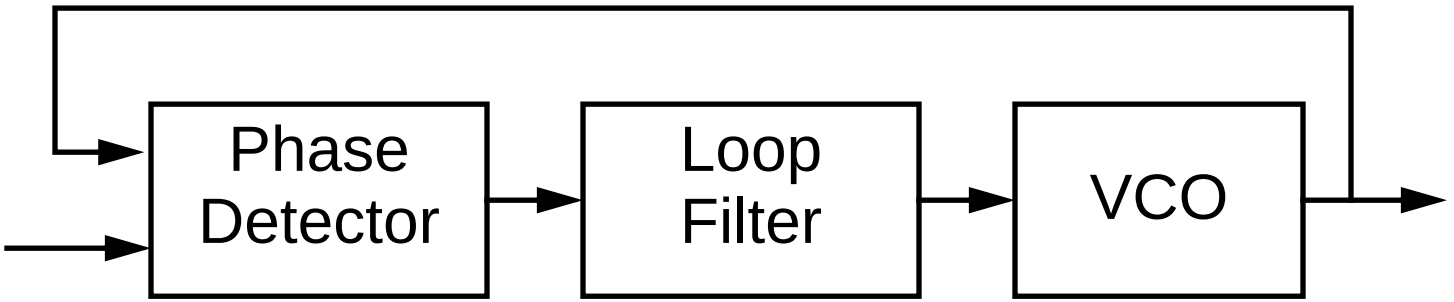
$$x(t) = A\cos\omega_c t$$

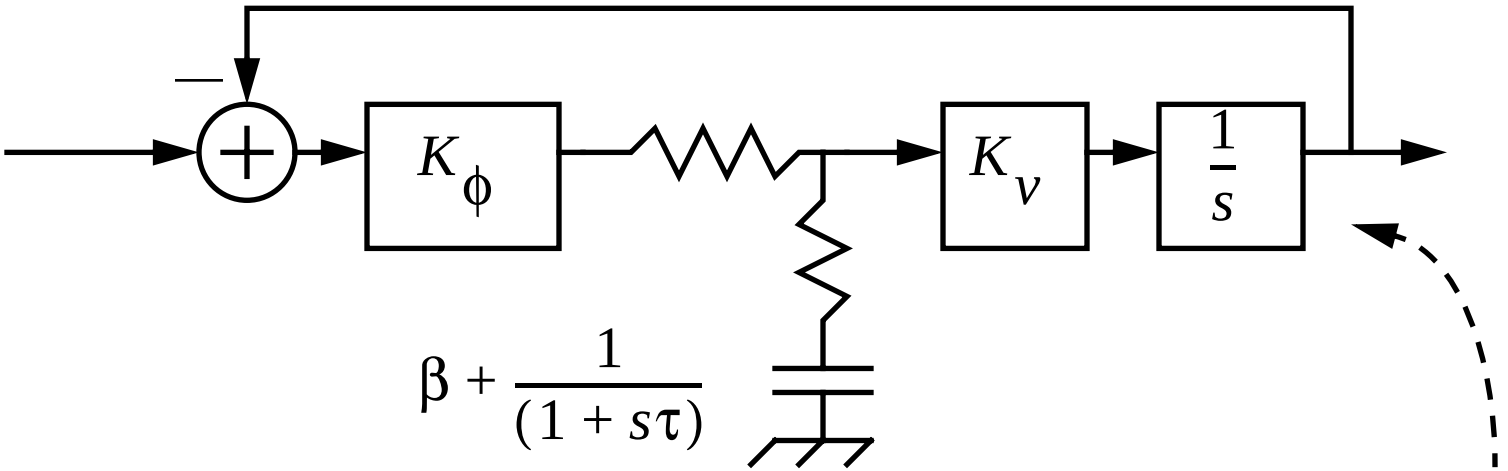
Jittered Clock:

$$x(t) = A\cos[\omega_c t + \phi(t)]$$

$\phi(t)$ is then treated as a continuous time signal

Model of Loop

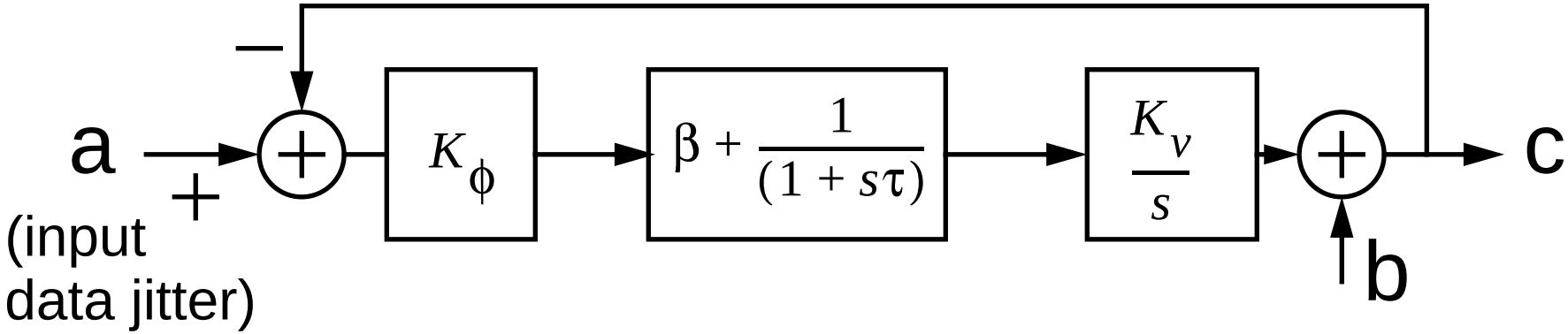


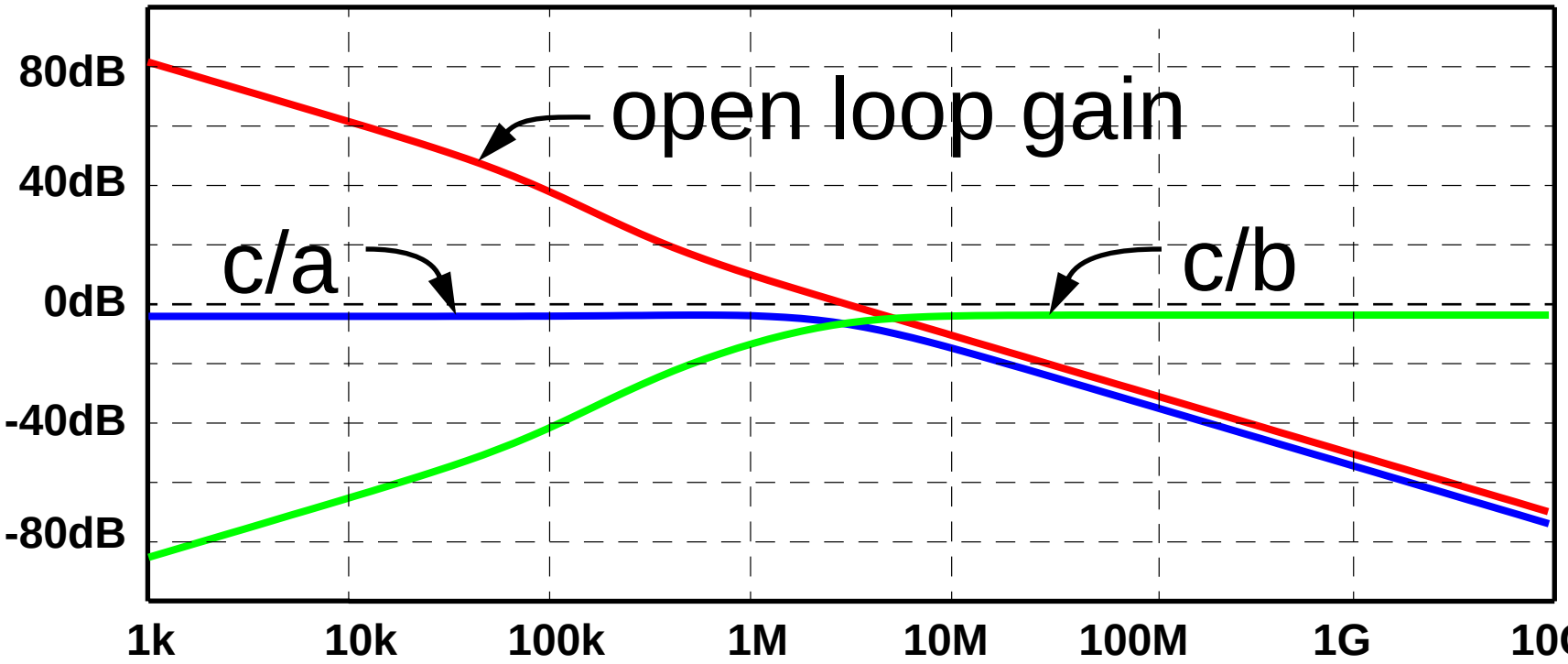


Warning: Extra Integration in loop makes for tricky design!

See Floyd M. Gardner, “Phaselock Techniques”, John Wiley and Sons, for good introduction to PLL theory

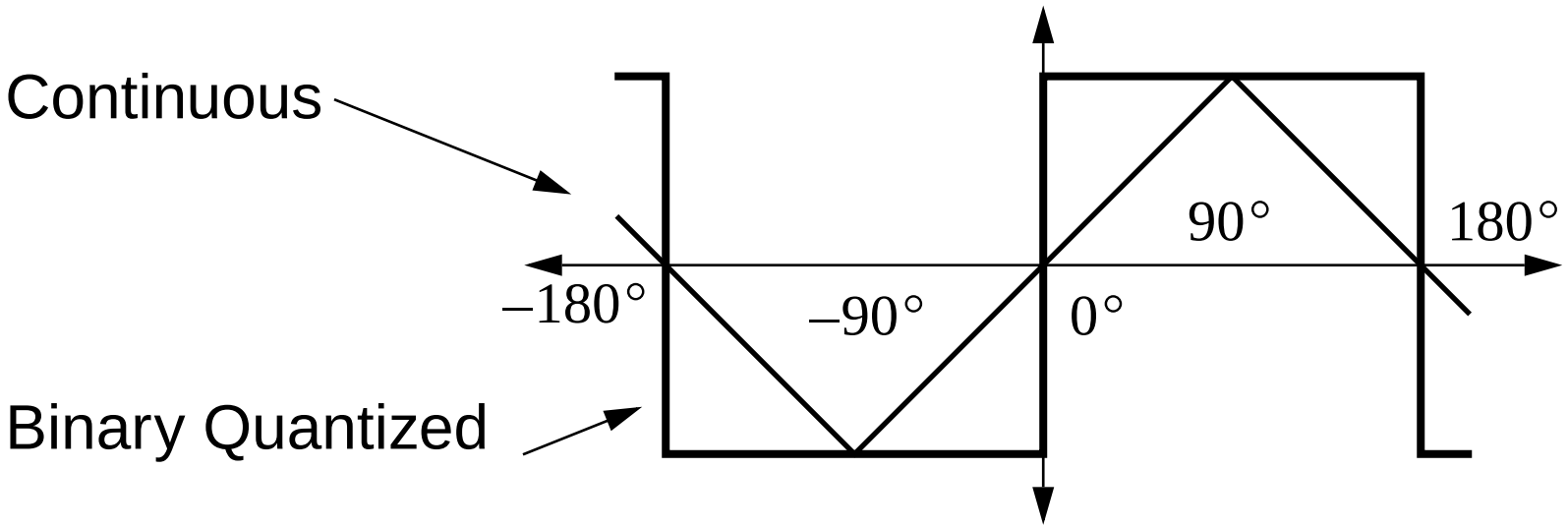
Loop frequency response





Phase Detectors

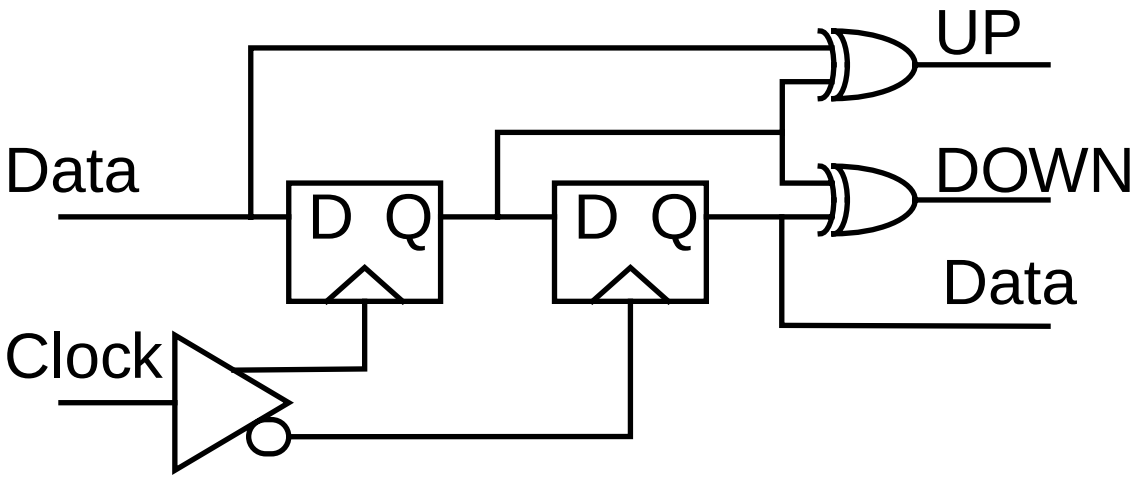
- Phase detectors generate a DC component proportional to deviation of the sampling point from center of bit-cell
- Phase detectors are:



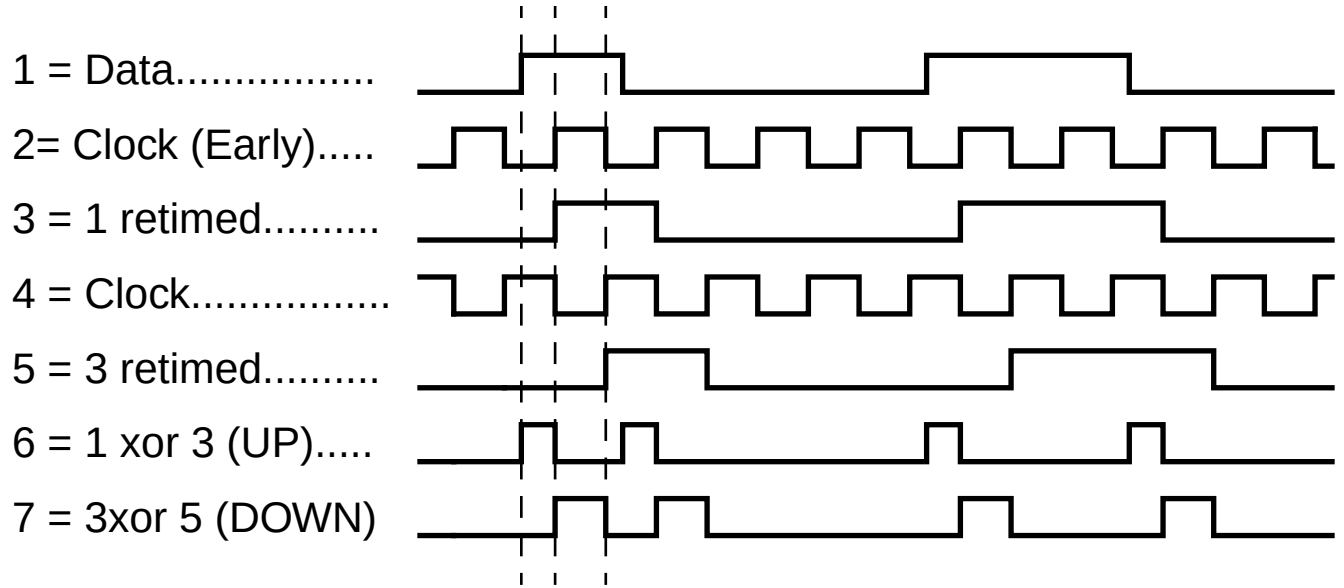
- Binary quantized phase detectors are also called “Bang-bang” phase detectors

After Tom Hornak: “Interface Electronics for Fiber Optic Computer Links”, (see bibliography for full citation)

“Self-Correcting Phase Detector”

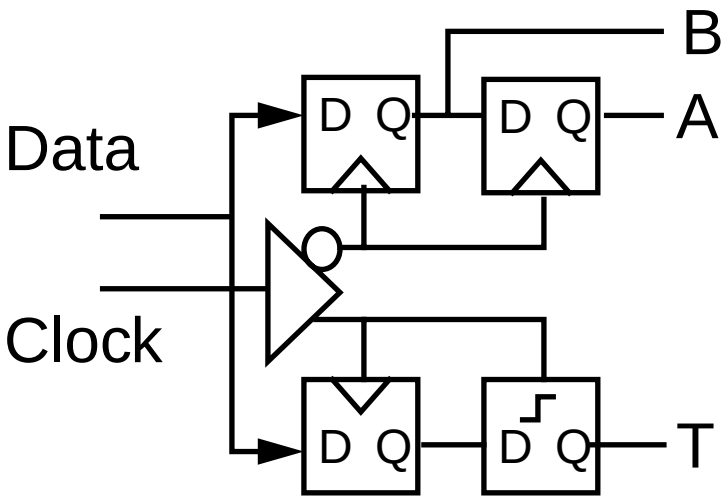


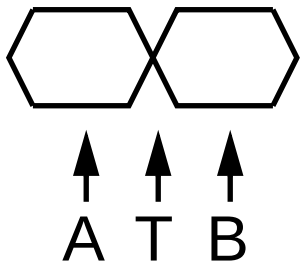
[Hog85][Shi87]



Binary Quantized Phase Detector

- NRZ data is sampled at each bit cell and near the transitions of each bit cell
- The sign of the transition sample is compared with the preceeding and following bit cell sample to deduce the phase error





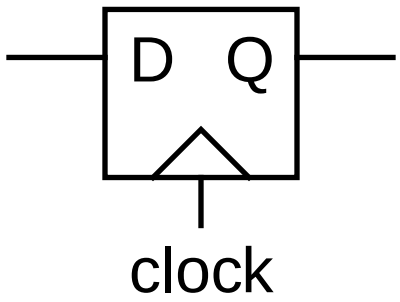
A	T	B	Output
0	0	0	tristate
0	0	1	vco fast
0	1	0	?
0	1	1	vco slow
1	0	0	vco slow
1	0	1	?
1	1	0	vco fast
1	1	1	tristate

[Ale75][WHY91][LaW91][ReG73]

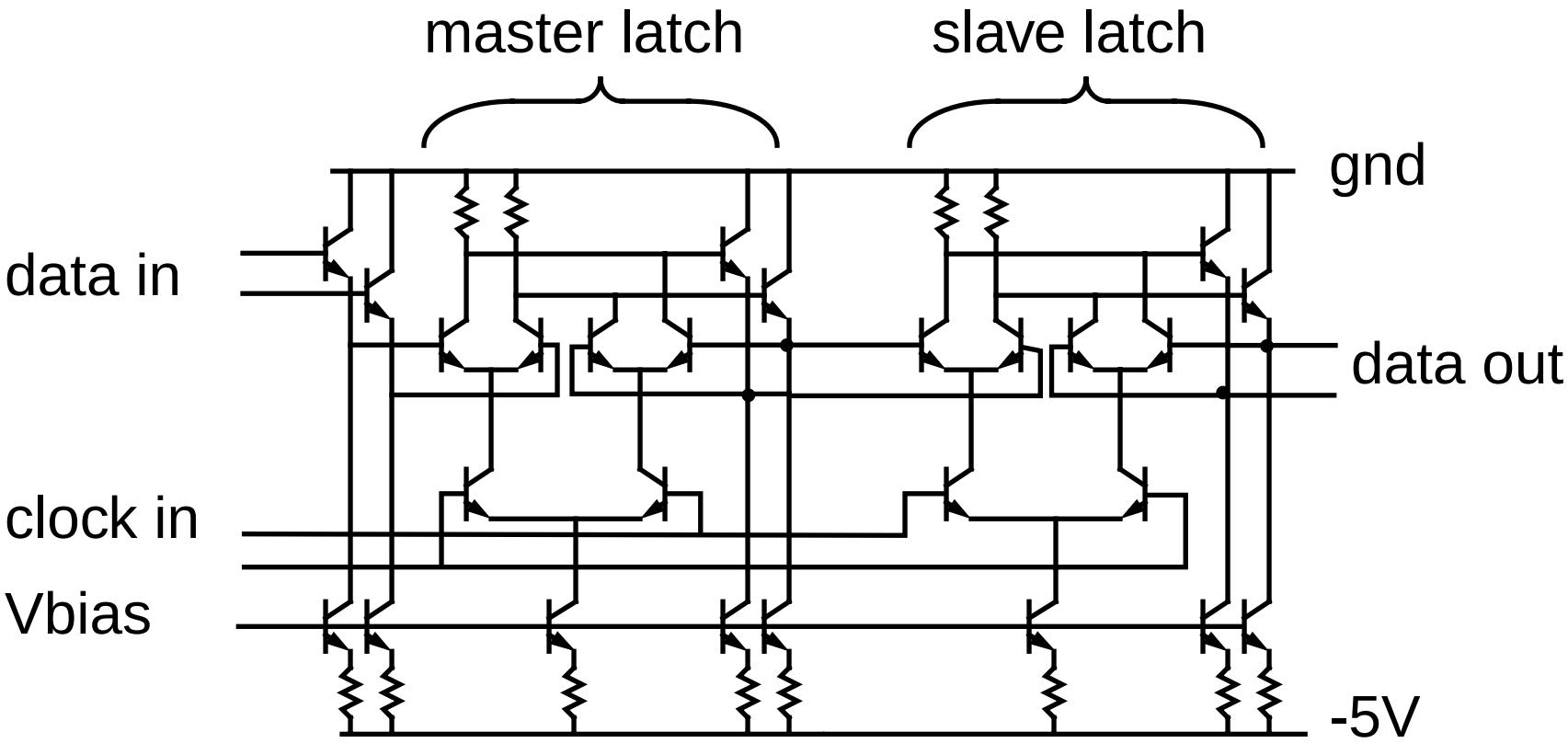
Decision Circuit

- Quantizes amplitude at precise sample instant
- Typically uses positive feedback to resolve small input signals
- A master/slave D-flip-flop carefully optimized for input sensitivity and clock phase margin is a common choice
- Latches data on the rising edge of clock signal

simplified schematic symbol:



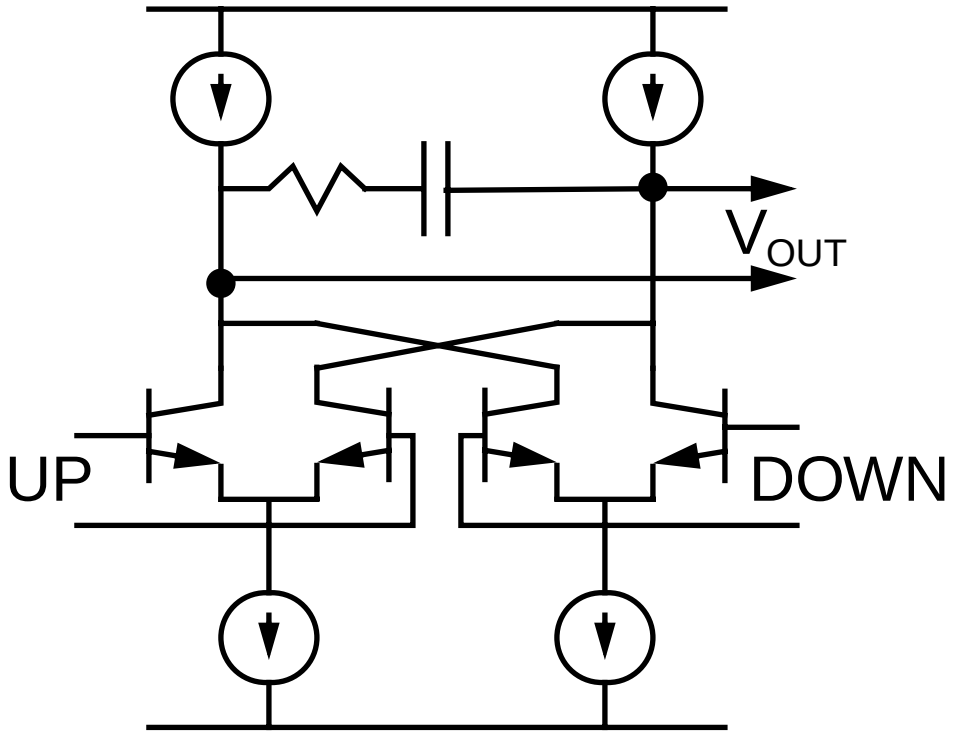
Example Bipolar Decision Circuit



- many clever optimizations are possible

[OhT83][Con84][Lai90][Run91][Hau91][Run91]

Loop Filters

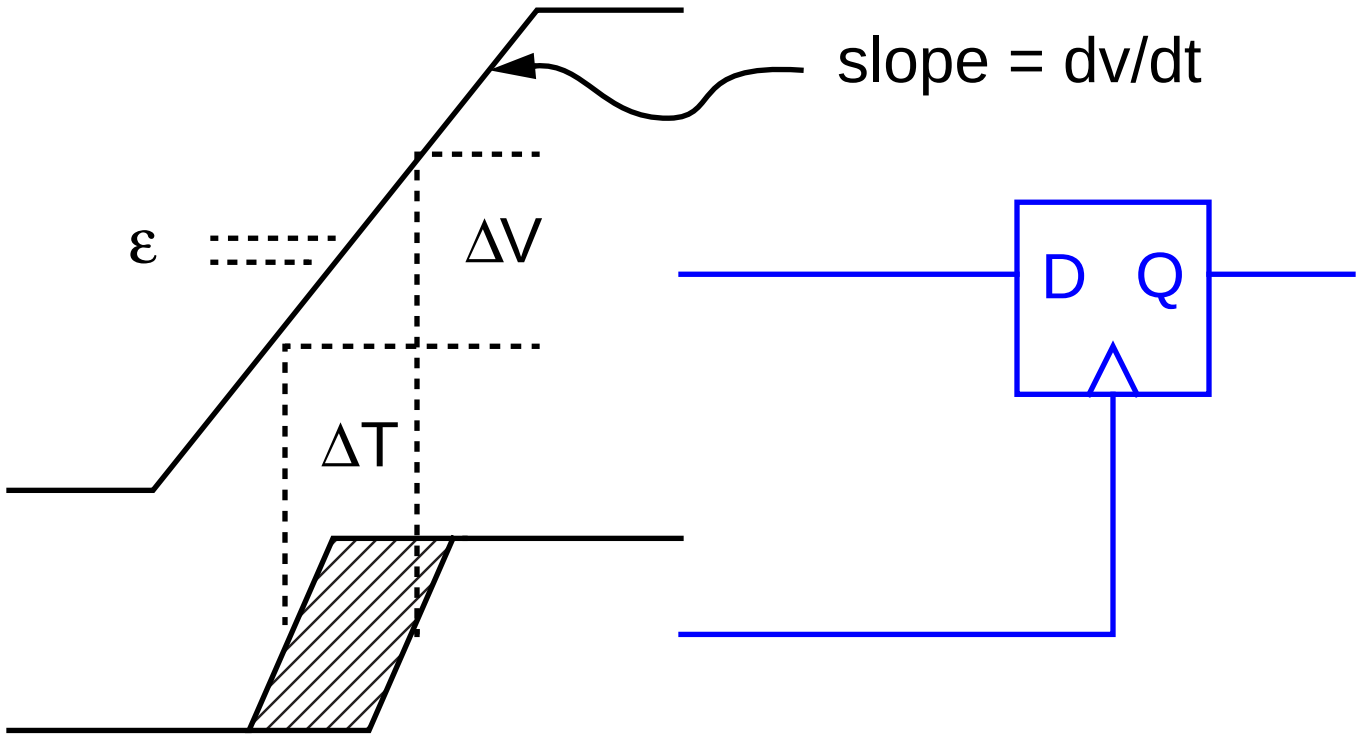


[Den88] [Dev91]
[LaW91] [WuW92]

UP	DOWN	V_{OUT}
0	0	tristate
0	1	ramp DOWN
1	0	ramp UP
1	1	tristate

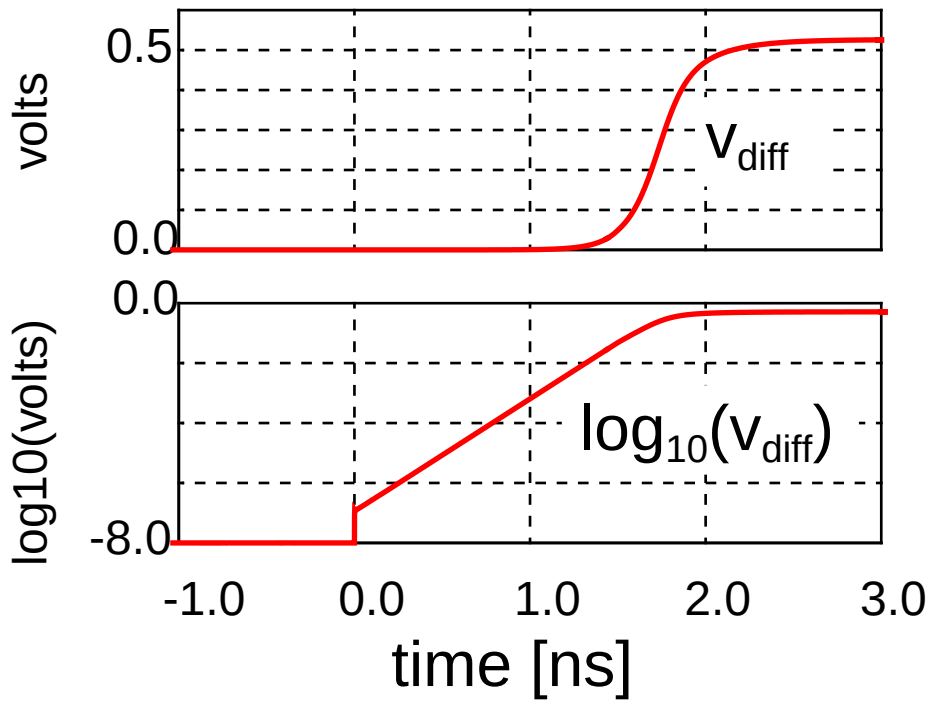
- should have provision for holding value constant (tri-stating) under long run-length conditions
- may be analog (integrator) or digital (up-down counter) - but *watch out for metastability*!

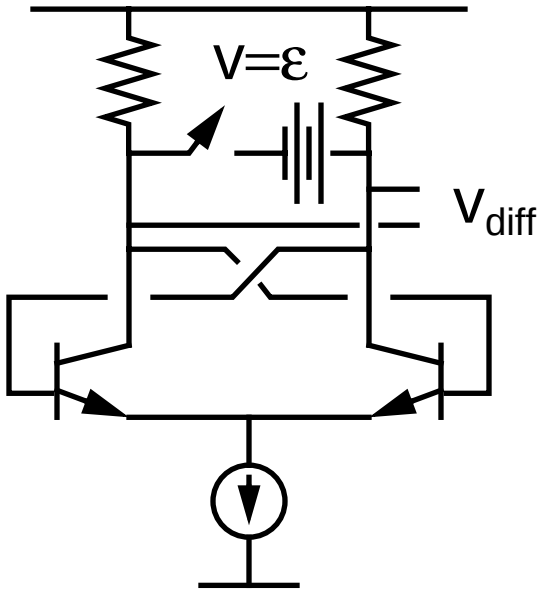
Metastability



For uniform clock jitter, and a latch “danger zone” of ε, the metastability probability $p_{metastability}$, is $\frac{\varepsilon}{\Delta T} \cdot \frac{dt}{dv}$.

Regeneration time constant τ



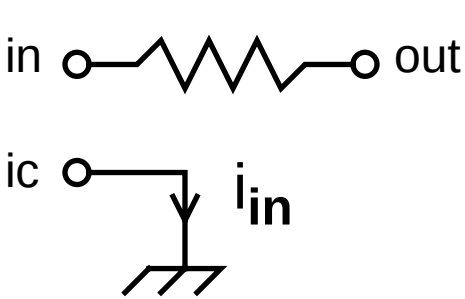


A small voltage ε is forced on latch, until t=0. Differential voltage V_{diff} grows as $\varepsilon \cdot e^{t/\tau}$. For a given V_{min} and ε, the regeneration time required is $\tau \cdot \log\left(\frac{V_{min}}{\varepsilon}\right)$.

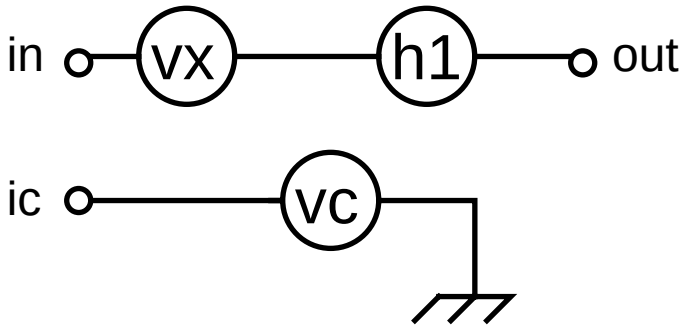
SPICE tip: current-controlled R/switch

```
# SPICE time variable resistor.
# the resistance between %in and %out is numerically
# equal to the current pulled out of %ic

.SUBCKT tvres %in %out %ic
h1 %inx %outx poly(2) vx vc 0 0 0 0 1
rdamp %out %outx 0.001
vx %inx %in 0
vc %ic 0 0
.ENDS
```

$R = i_{in} * 1\ \Omega/A$



v(h1)=i(vx)*i(vc)*1 Ω/A



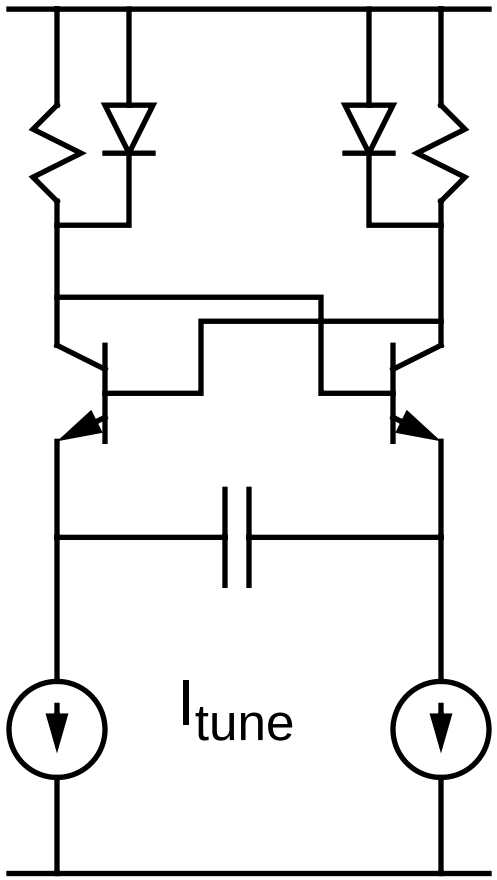
VCO alternatives

	LC Oscillator	**Multivibrator**	**Ring Oscillator**
Speed	Technology Dependent 1-10's of GHz, CMOS 1-2 GHz		
Phase Noise	Good	Poor	
Integration	Poor (L, Varactor)	Excellent	
Tunability	Narrow/Slow	Wide/Fast	
Stability	Good	Poor (needs acquisition aid)	
Other			Multi-Phase Clocks

- [Cor79, Ena87, Wal89, DeV91, Lam93, WKG94]

After Todd Weigandt, B. Kim, P.Gray, "Timing Jitter Analysis for High-Frequency CMOS Ring Oscillators", March 10, 1994

Multivibrator VCO



Capacitor is alternately charged and discharged by constant current

Tuned by varying I_{tune} in current source

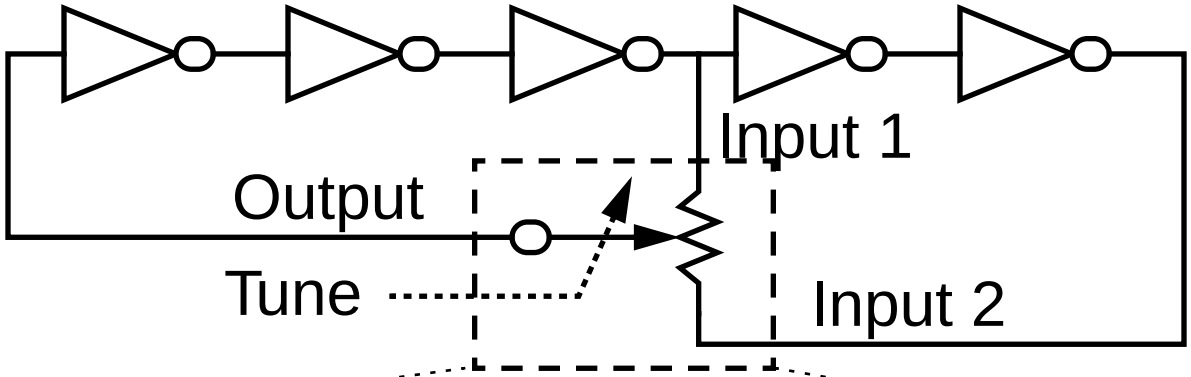
Diode clamps keep output voltage constant independent of frequency

Relies on non-linear switching for oscillation behavior, and so is limited to moderate frequencies.

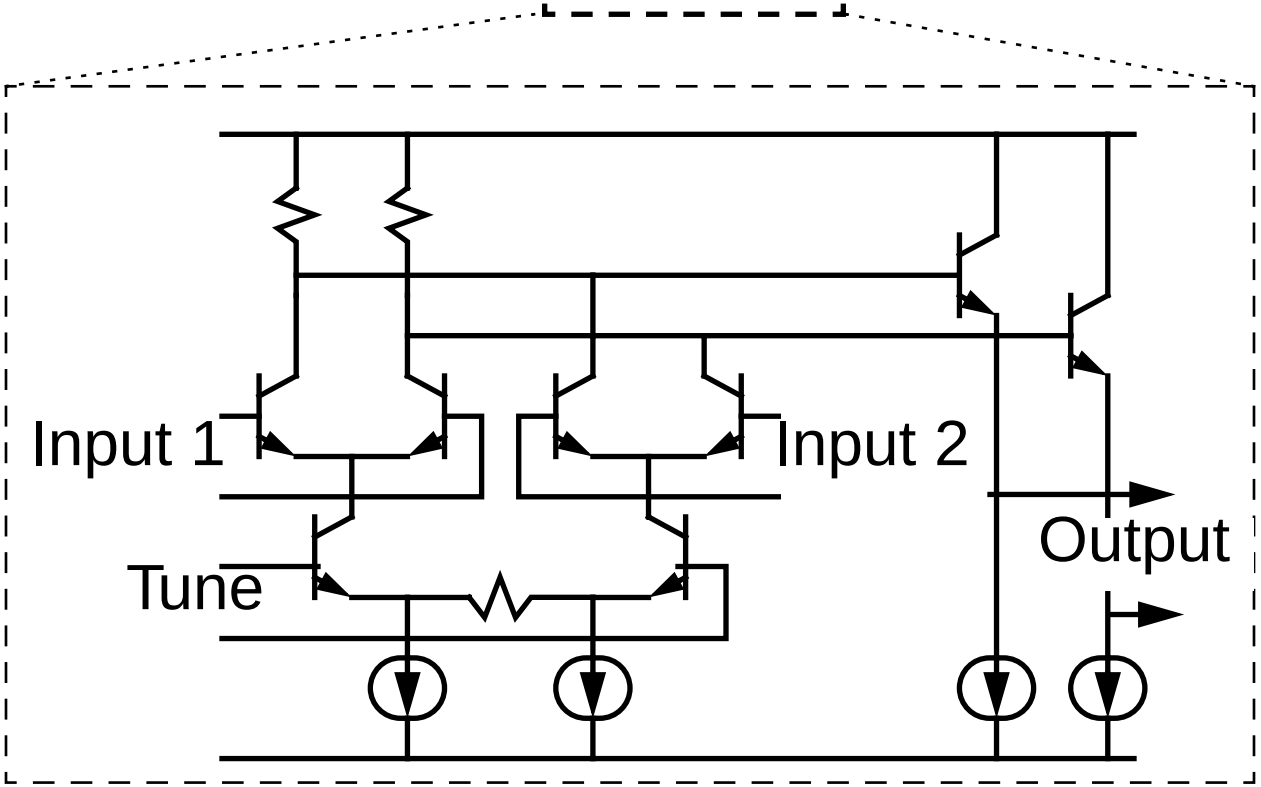
Frequency = $\frac{I_{tune}}{4CV_{be}}$

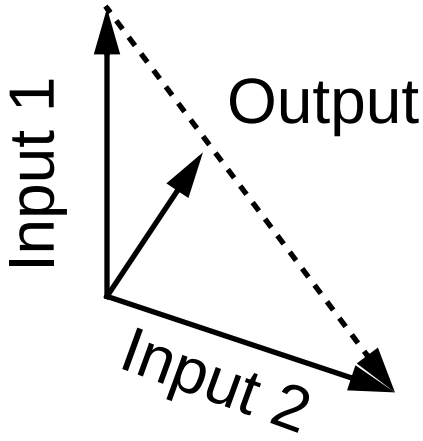
After Alan B. Grebene, “Analog Integrated Circuit Design”, Van Nostrand Reinhold, 1972, pp 313-315

Example Ring Oscillator VCO

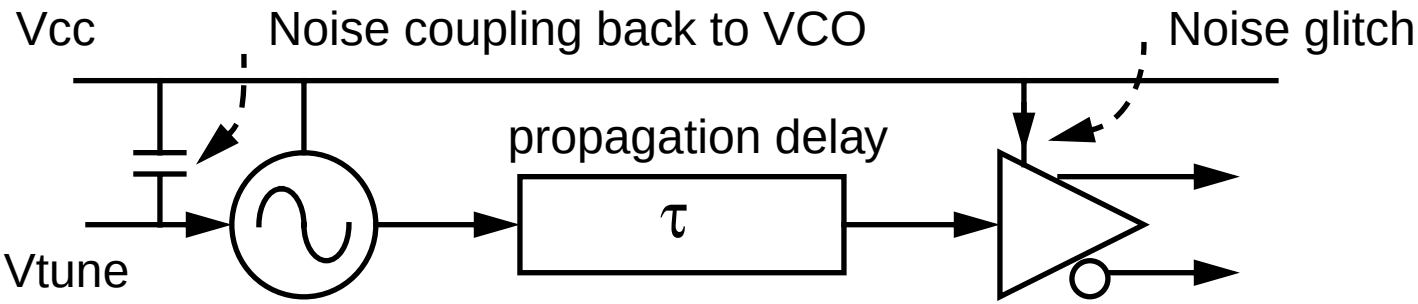


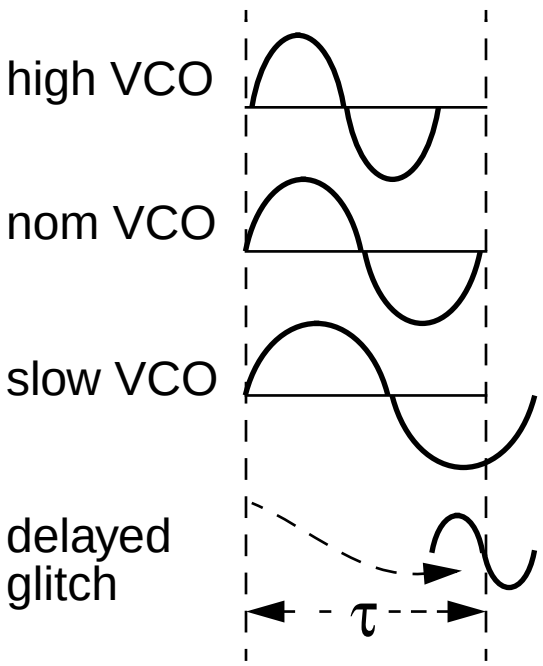
[SyA86]
[EnA87]
[Wal89]





VCO injection locking (problem)





most VCO's *sample* the tune voltage once per cycle - down converting the system noise.

- PLL: $F_{osc} \alpha V_{tune} \alpha \overline{\theta_{error}}$
- ILO: $F_{osc} \alpha V_{tune} \alpha \theta_{error}$

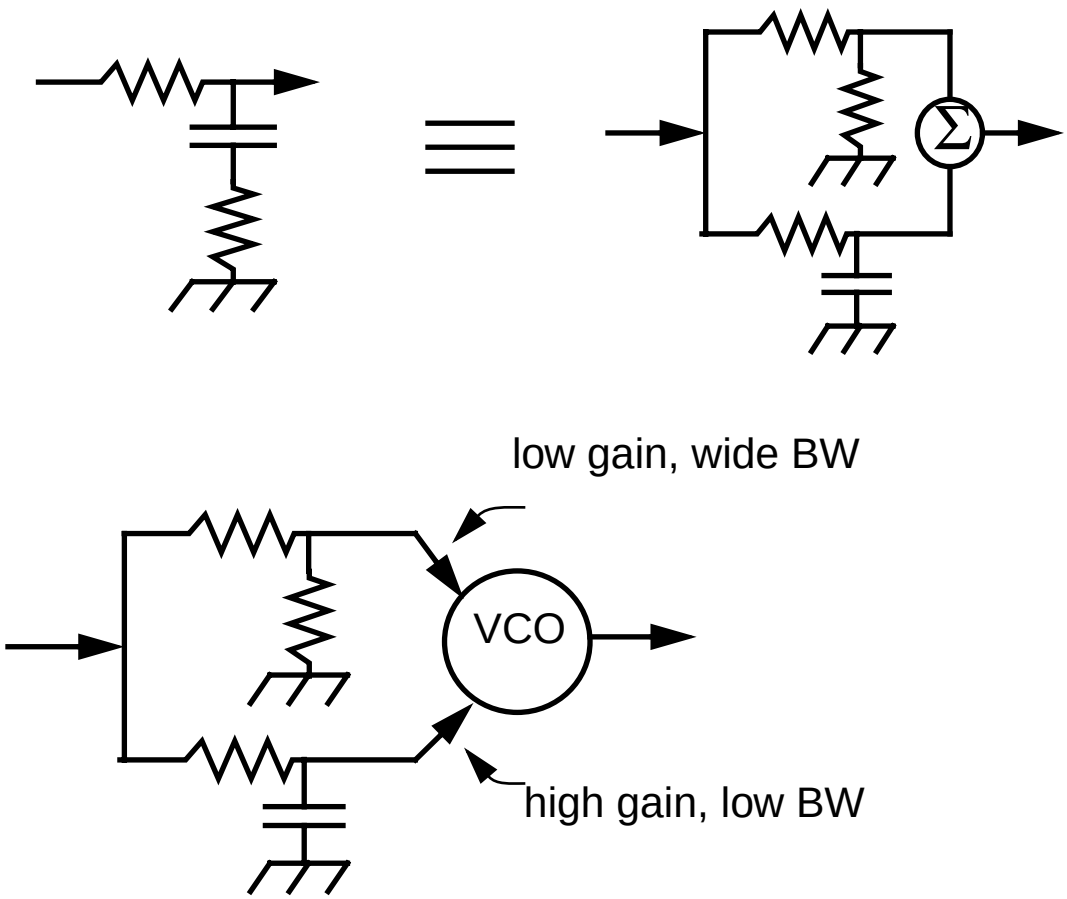
VCO can *injection lock* to its own delayed signal more rapidly than to input data!

VCO injection locking (a solution)

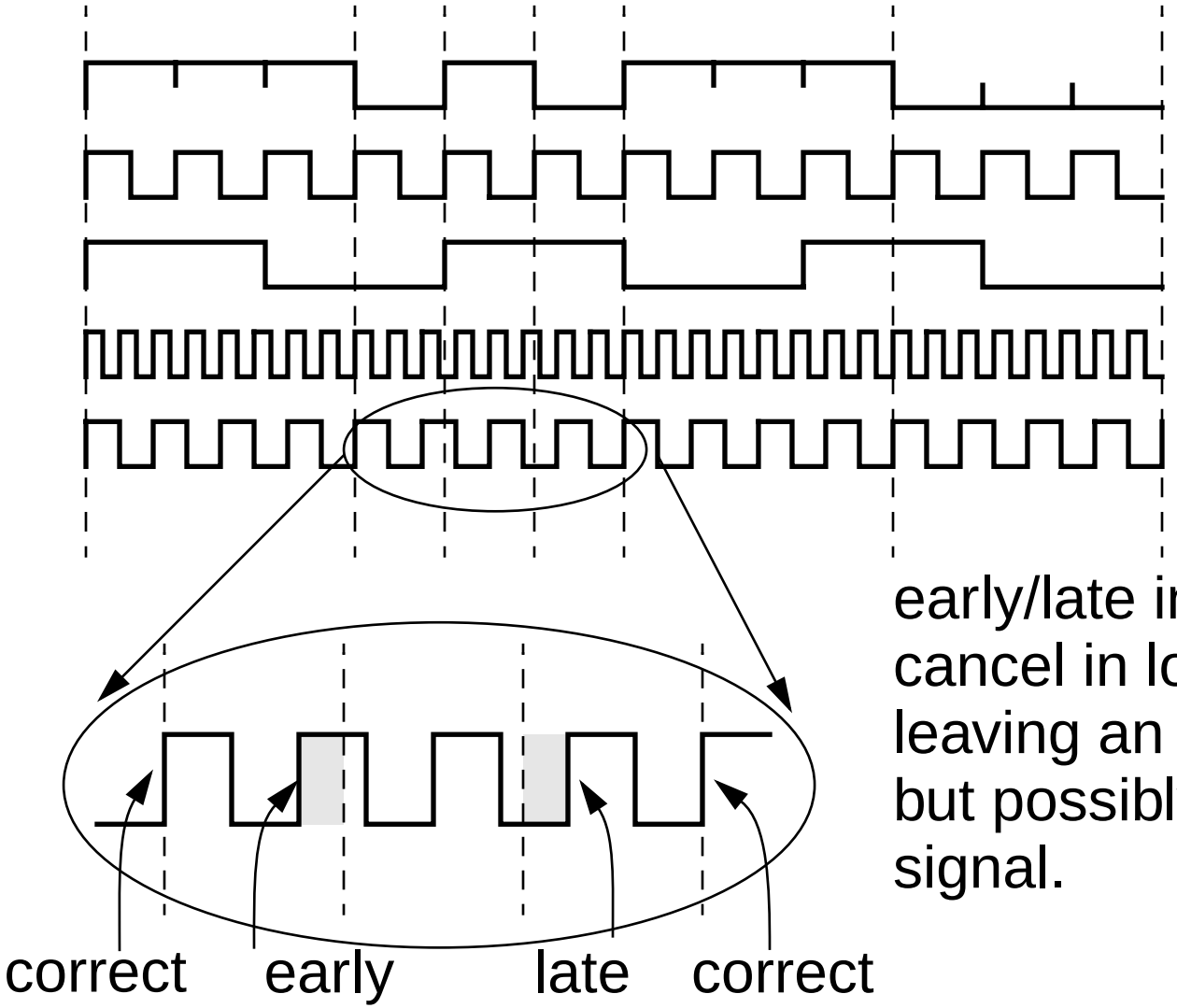
Decompose the loopfilter pole/zero into two separate tuning inputs:

- a wide range input with very low bandwidth
- a narrow tuning range input with wide BW.

this greatly reduces effect of VCO noise on tuning curve.



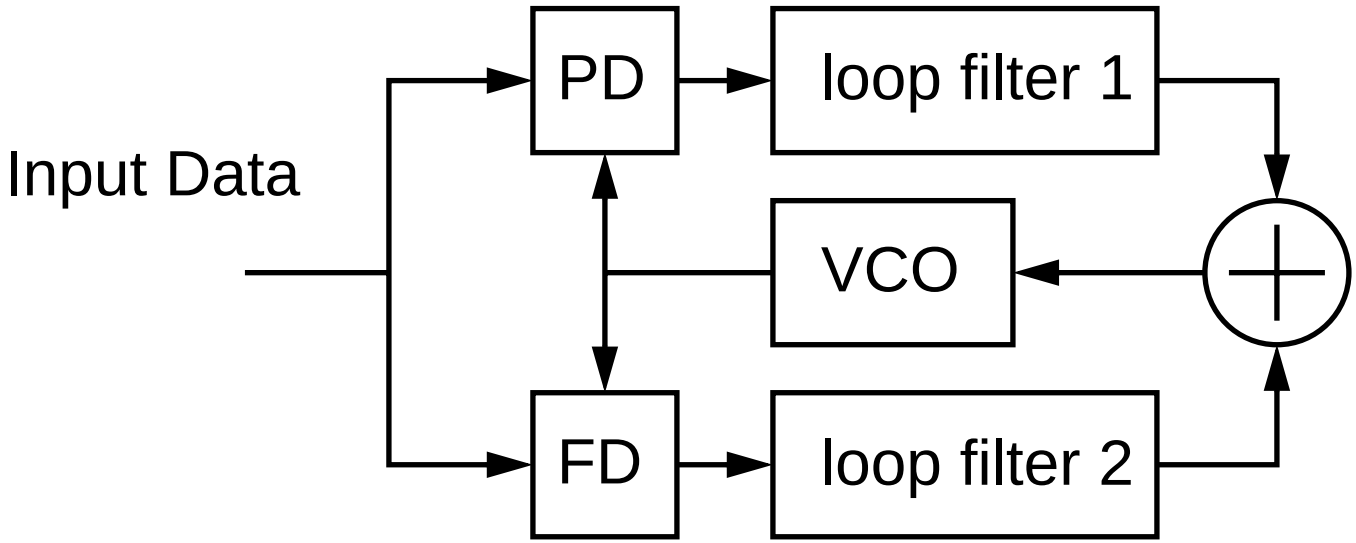
False or Harmonic Locking to Data



early/late indications cancel in loop filter, leaving an attenuated, but possibly stable lock signal.

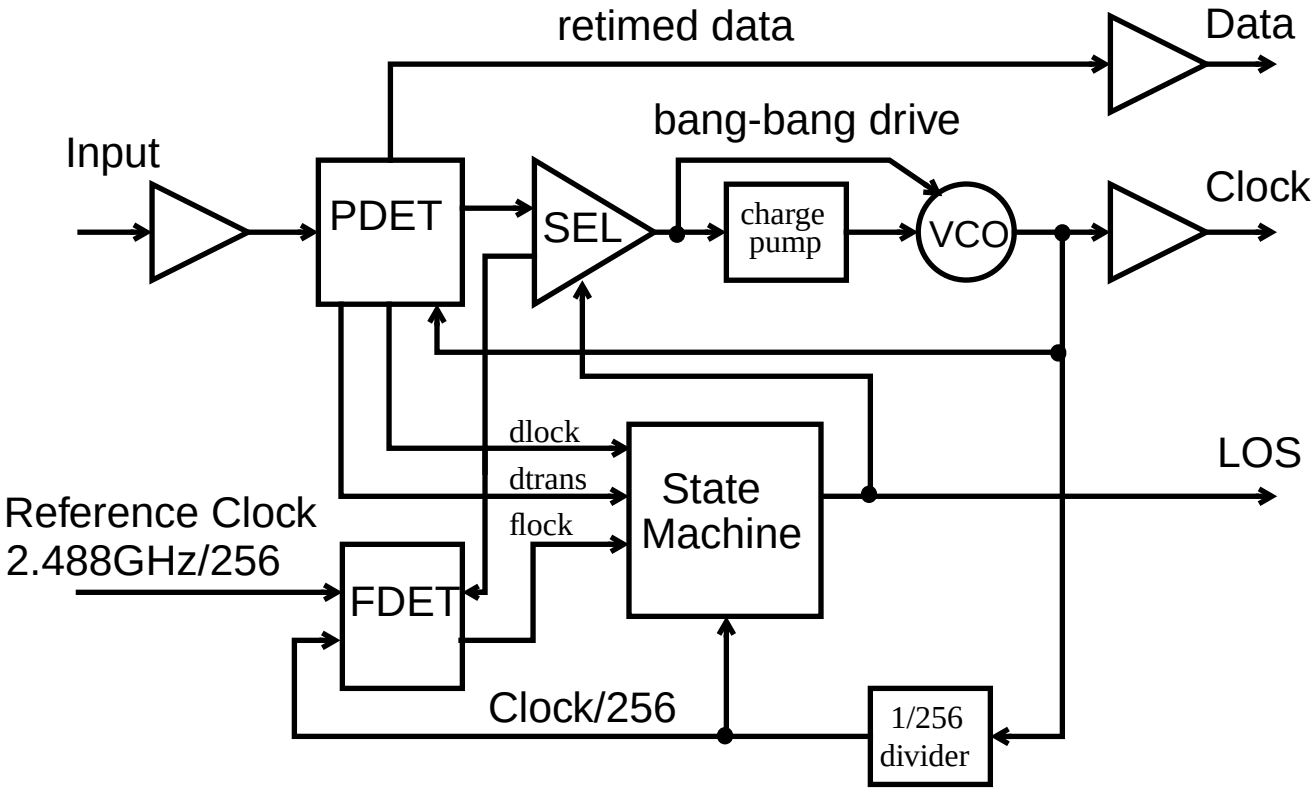
Aided Acquistion

- Tricky task due to Nyquist sampling constraints caused by stuttering data transitions



- Still subject to false lock if VCO range is too wide

Training Loops

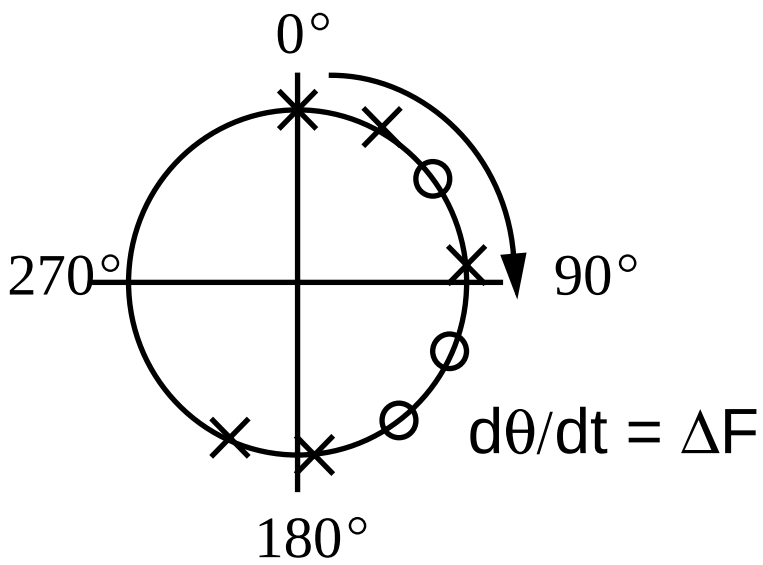


[WSY97]

An increasingly common technique is to provide a reference clock to the CDR circuit. This allows the VCO process-variation to be dynamically trimmed out, avoiding false locking problems.

Phasor Diagram

- Graph of relative phase between clock and data
- Each complete rotation is 1 unit interval of phase slip
- Rotations/second = frequency error (in Hz)



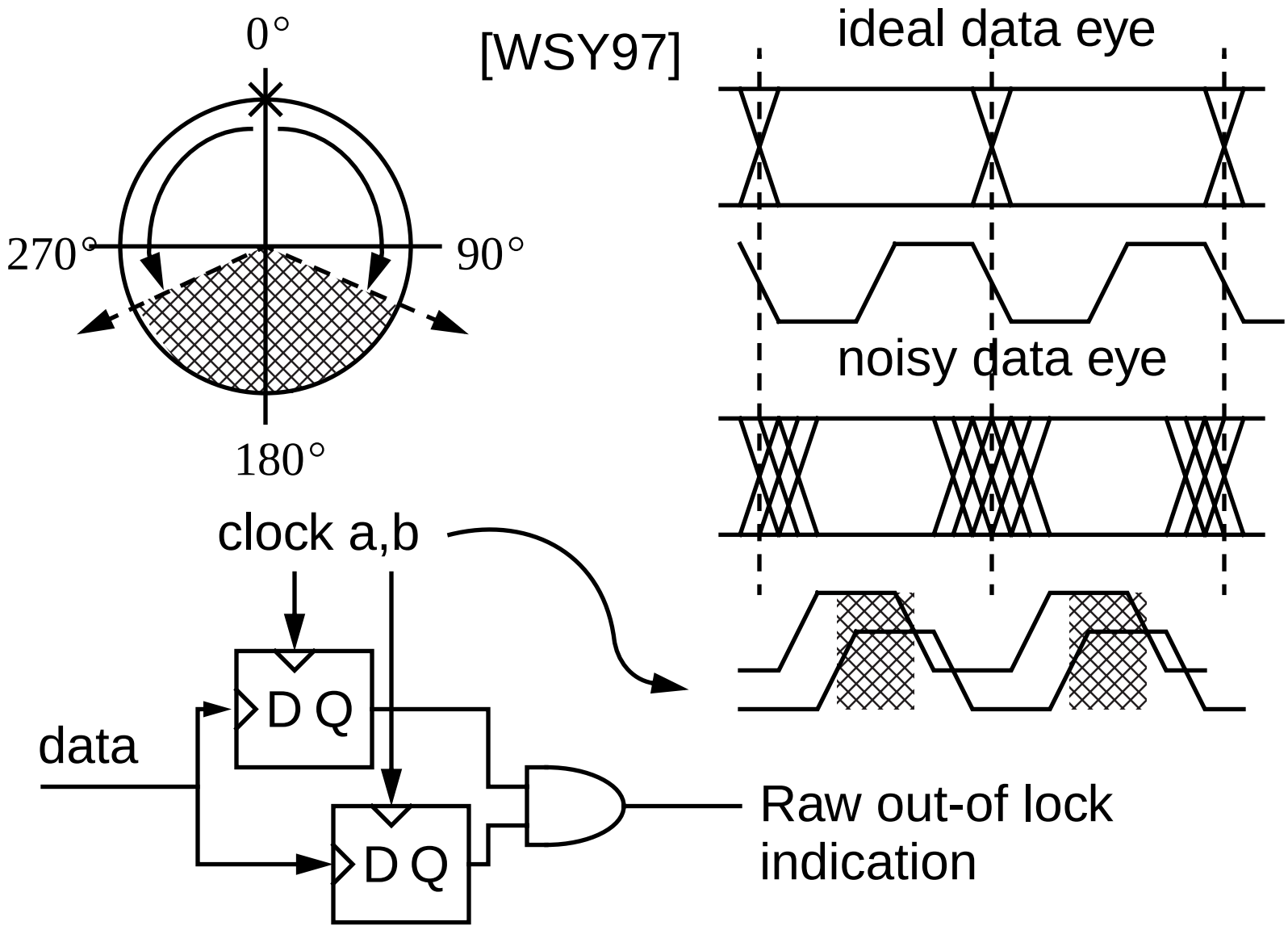
Plot of data transitions versus VCO clock phase.

Data at 1/2, or VCO at 2x, the proper frequency look locked. This puts a limit on VCO tolerance to prevent false locking.

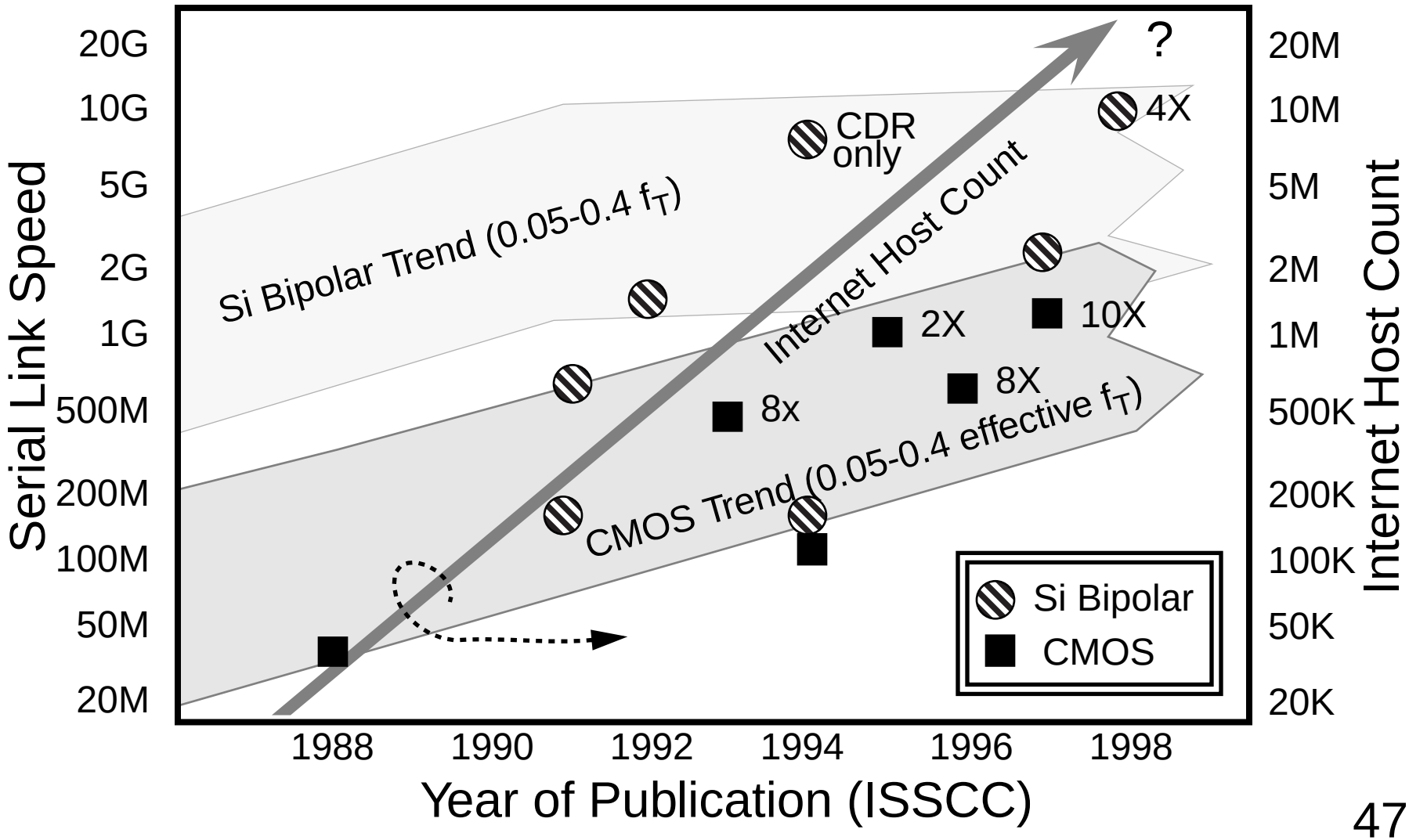
○ = missing transitions

× = actual transitions

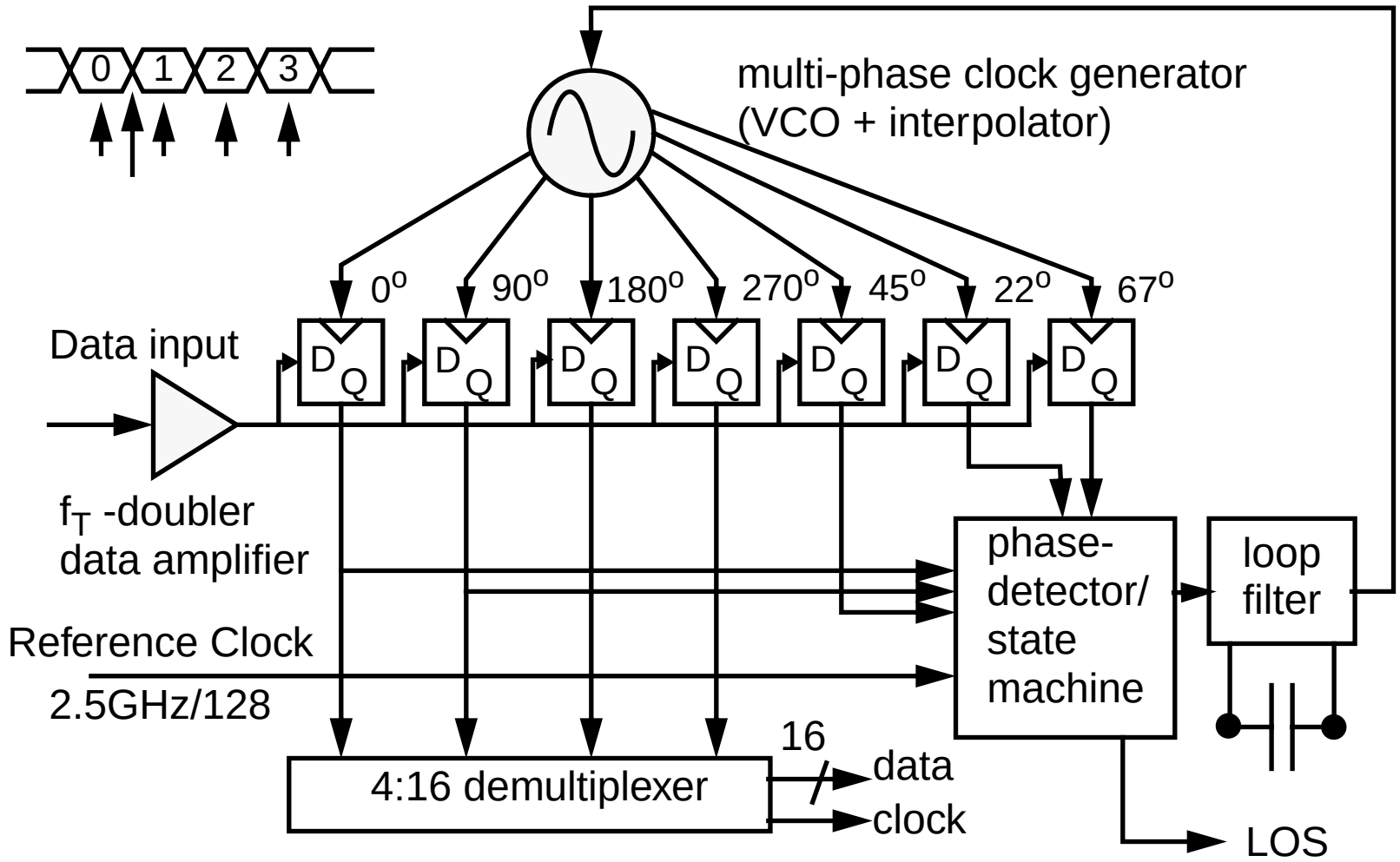
Example Lock Detector



Communication Trends



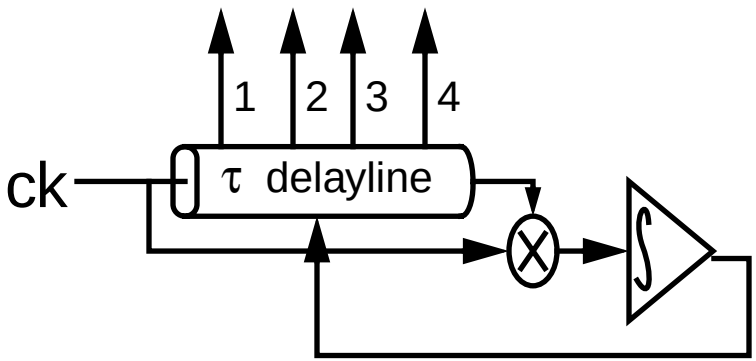
Multiphase Receiver Block Diagram



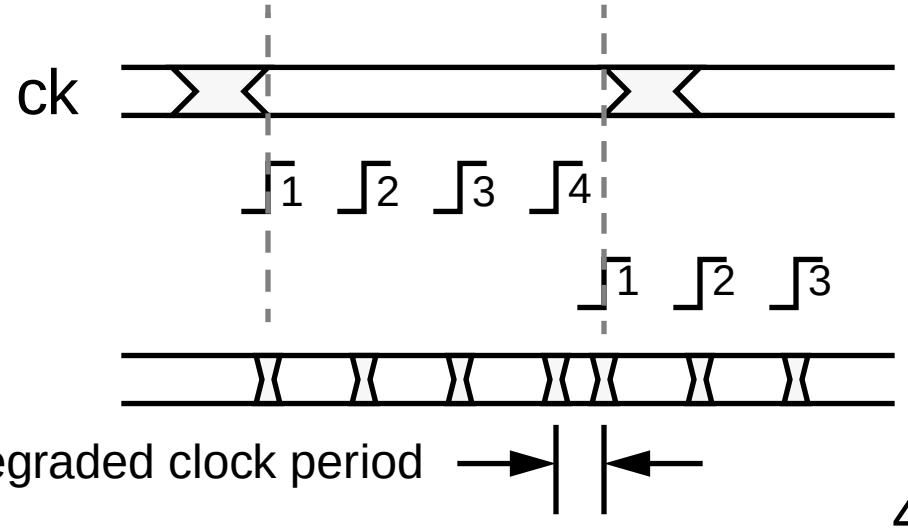
[WHK98]

DLL vs PLL which is “best”?

- DLLs do not filter input reference jitter, but do not accumulate VCO phase errors - best for clock synthesizers running from clean reference.
- PLLs can have higher phase noise because of multiple passes through the delay gates of VCO, however is able to filter noisy input signals.



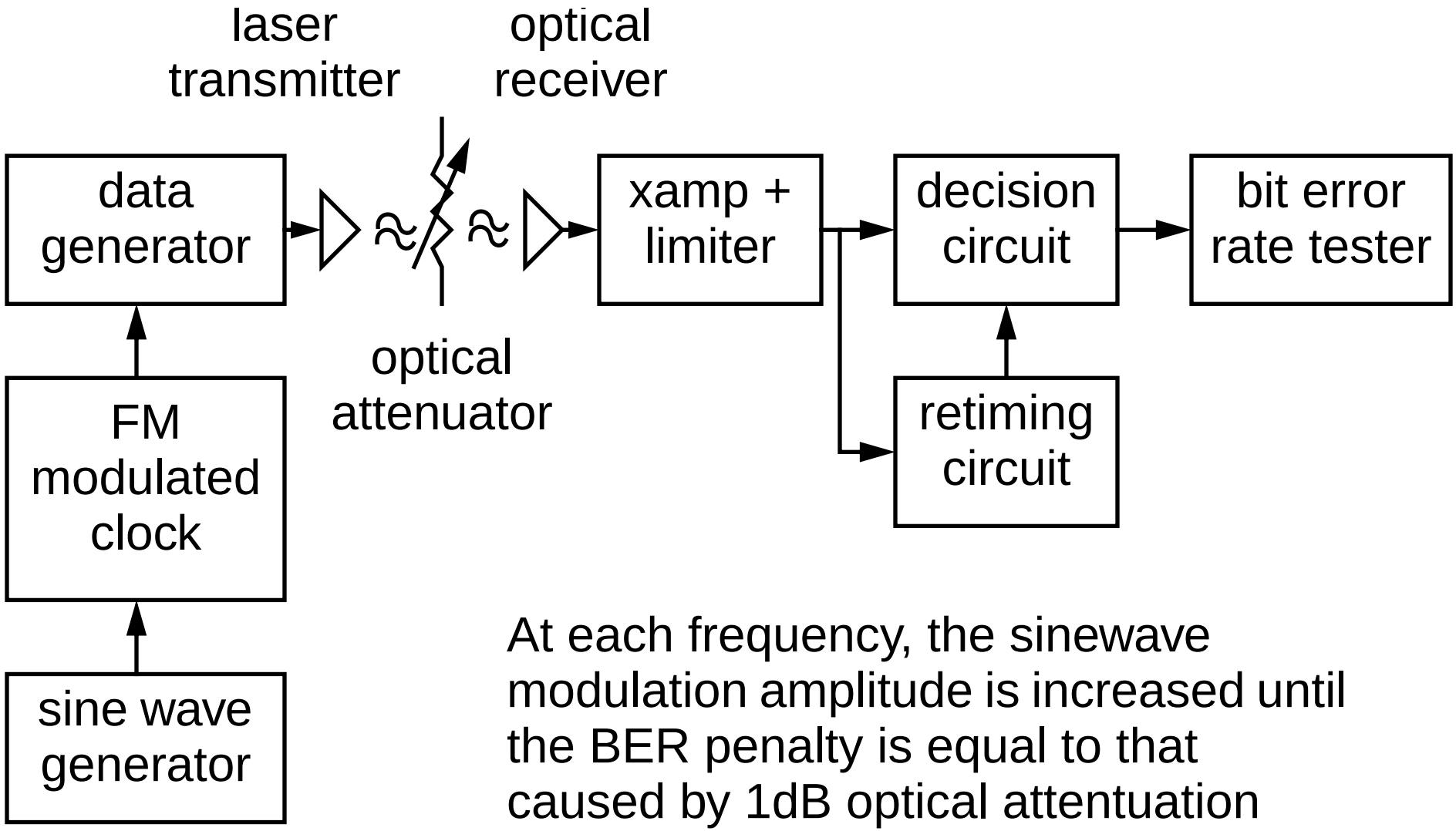
[KWG94]



Jitter Measurements

- SONET has the most complete set of jitter measurement standards, but the techniques are useful and relevant for datacom applications also
  - Jitter Tolerance
  - Jitter Transfer
  - Jitter Generation

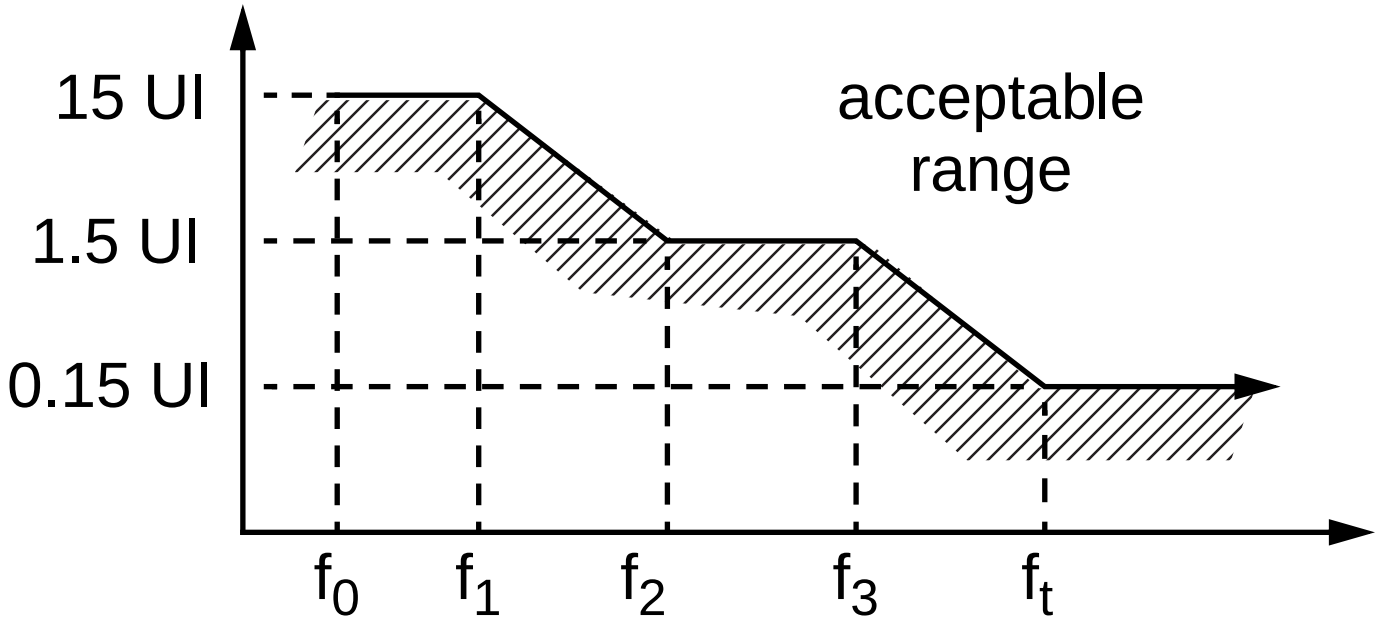
Jitter Tolerance Test Setup



At each frequency, the sinewave modulation amplitude is increased until the BER penalty is equal to that caused by 1dB optical attentuation

After Trischitta and Varma: “Jitter in Digital Transmission Systems”

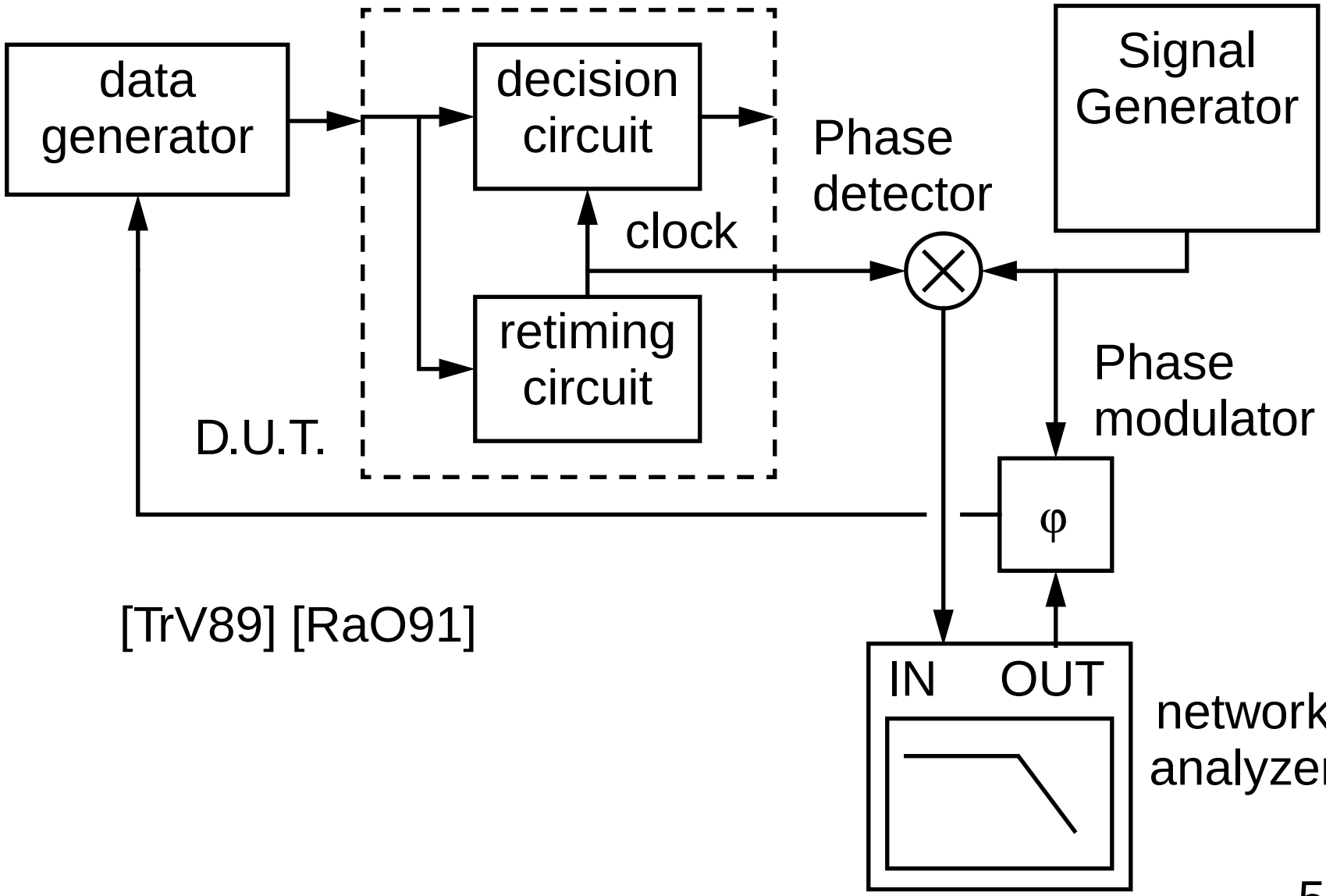
SONET Jitter Tolerance Mask



Data Rate	f_0[Hz]	f_1[Hz]	f_2 [Hz]	f_3 [kHz]	f_t [kHz]
155 Mb	10	30	300	6.5	65
622 Mb	10	30	300	25	250
2.488 Gb	10	600	6000	100	1000
10 Gb	?	?	?	400	4000

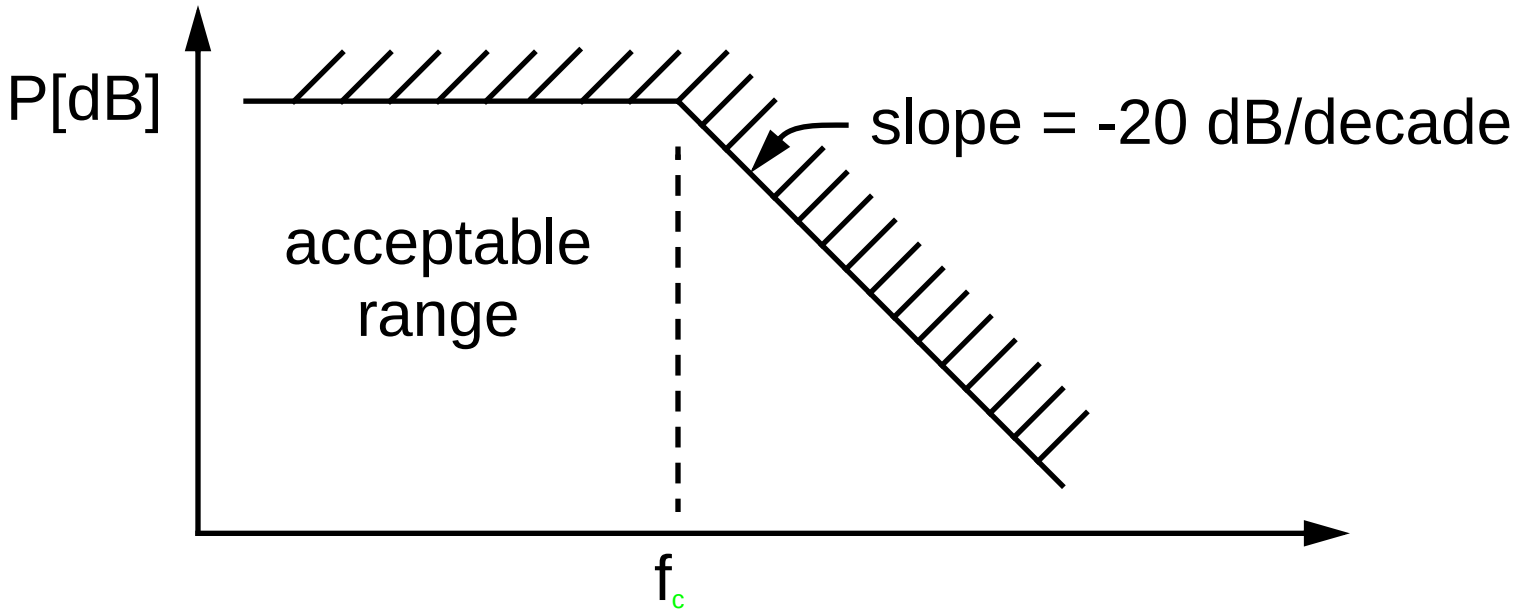
from SONET SPEC: TA-NWT-000253 Issue 6, Sept. 1990, fig 5-13

Jitter Transfer Measurement



[TrV89] [RaO91]

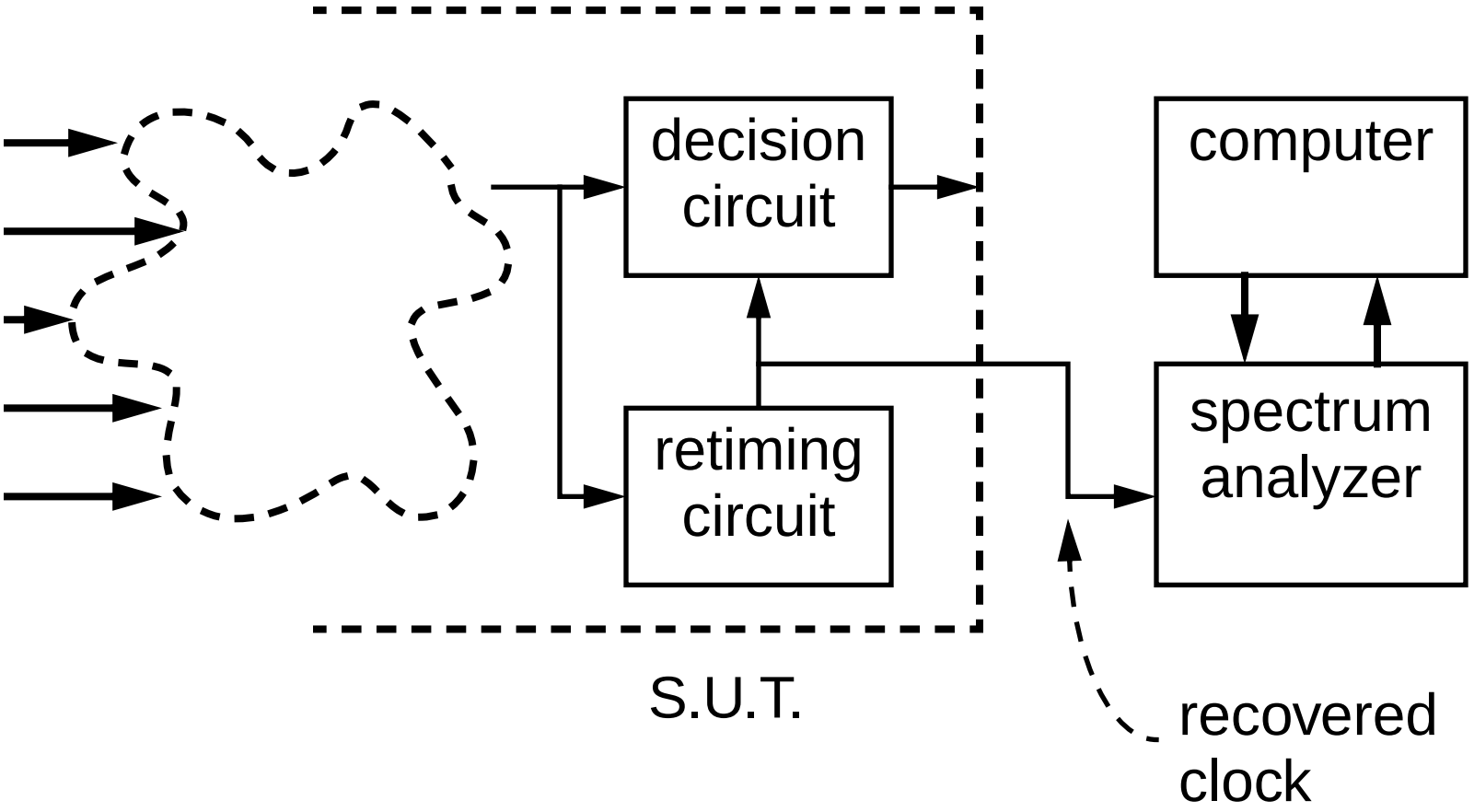
Jitter Transfer Specification



Data Rate	f_c[kHz]	P[dB]
155 Mb	130	0.1
622 Mb	500	0.1
2.488 Gb	2000	0.1

This specification is intended to control jitter peaking in long repeater chains

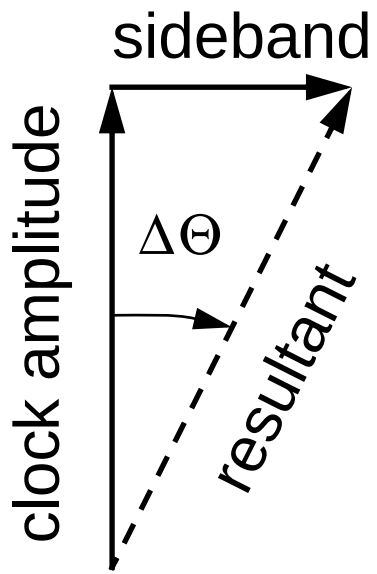
Jitter Generation



Jitter Generation (cont.)

1) Measure Jitter Sidebands around Clock

$$Jitter_{pp(rads)} = 2\Delta\Theta \cong 2\,\mathrm{atan}\left(\frac{V_{sideband}}{V_{clock}}\right)$$



2) Multiply Jitter components by Filter Mask

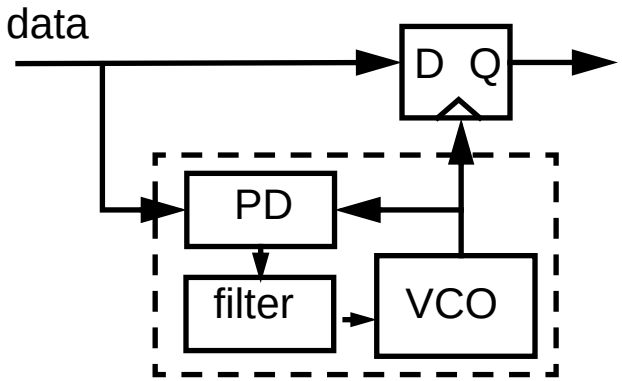
3) RMS sum total noise voltages over band

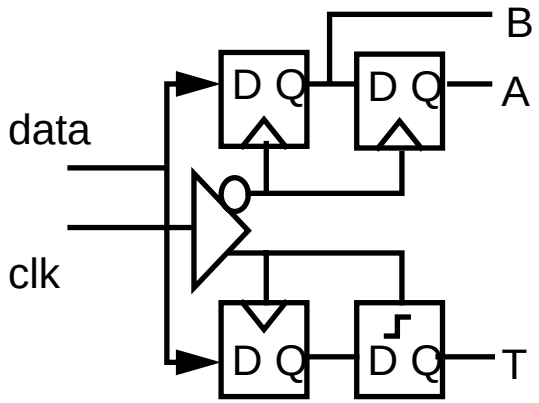
4) Convert RMS noise voltage to RMS jitter

OC-48 (2.488 Gb/s SONET) specifies 12 kHz hipass filter, and maximum 0.01 UI RMS integrated jitter.

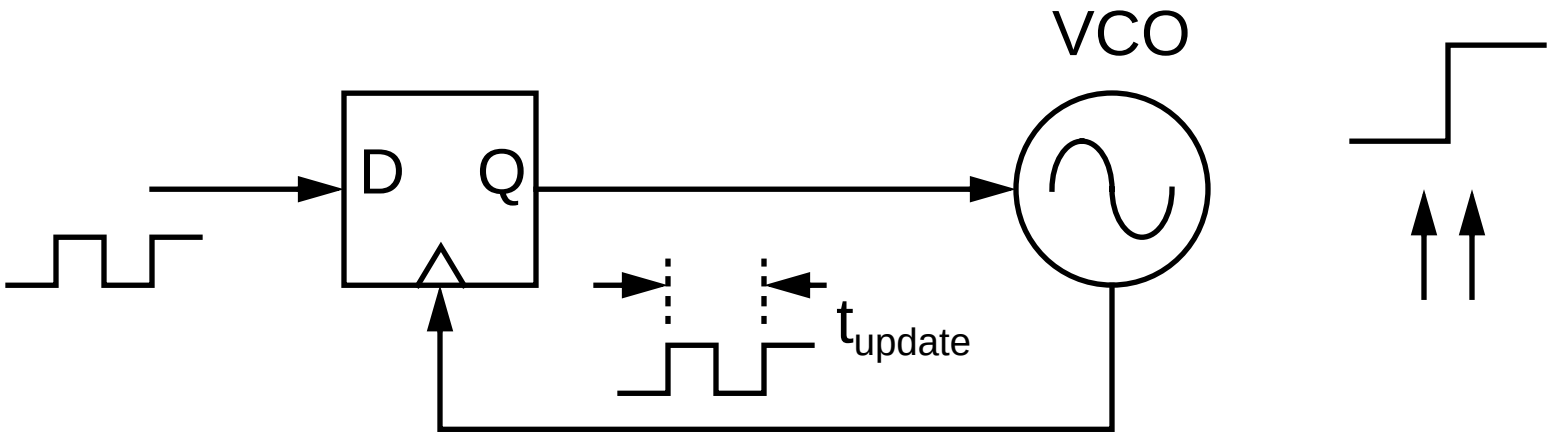
Why bother with a BB loop?

- it may be difficult to maintain optimum sampling point with traditional PD/PLL or with filter method over process, temperature and supply variation
- Narrow pulses of linear PD's may not work well at extremely high bit rates
- for monolithic implementation, BB PD has excellent match between retiming latch and PD latch - allows for operation at highest latch toggle frequency





Simple first-order BB loop



- VCO runs at two discrete frequencies: $f_{nom} \pm f_{bb}$.
- Phase error is evaluated at a discrete time interval t_{update}. In the general case, this can be considered approximately equal to mean transition time of the data.

How to simulate a loop?

- SPICE (boolean & polynomial)
- timestep simulator [FLS63]
- event driven simulator [Mac87]
- actual hardware

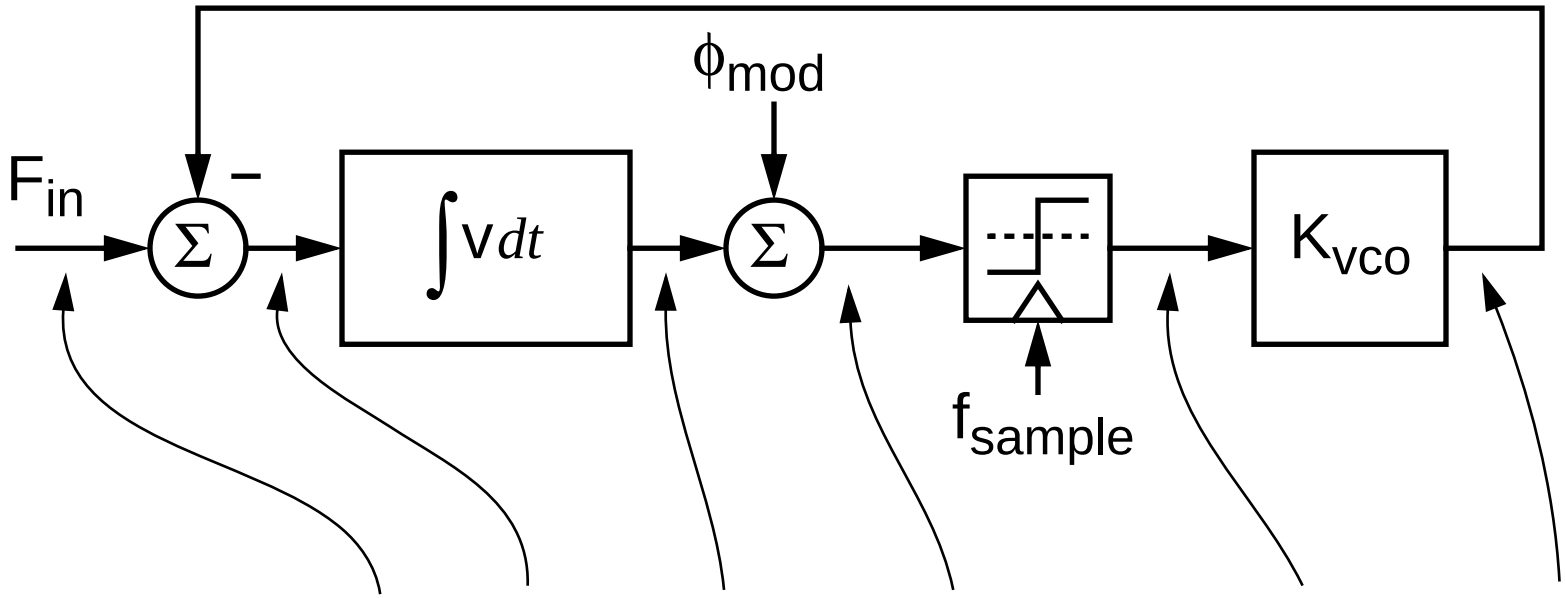
The need for *fast* simulation

- *understand* the design space
- check corner cases
- build intuition

Efficient Simulation Strategy

- Simulating VCO *waveform* is unnecessary to accurately model ideal PLL behavior.
- Only frequency and phase is needed.
- Model all circuit time-varying state variables as voltages.
- Convert between frequency and phase variables with explicit integration block.

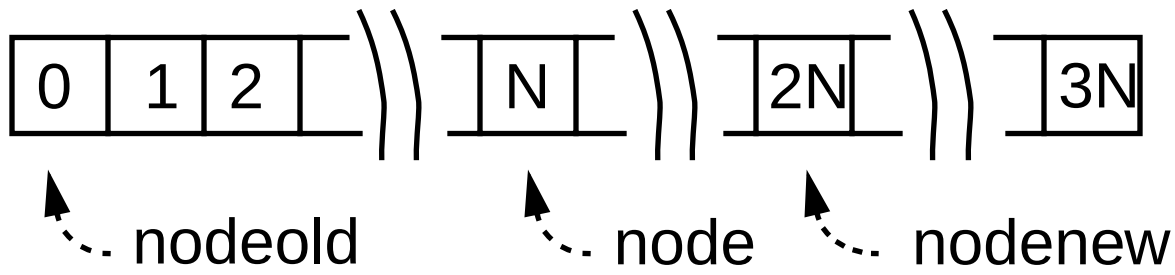
Model of First-order Loop



node:	F_{in}	ΔF	$\Delta\theta_1$	Θ_{error}	bbtune	F_{vco}
unit:	Hz	Hz	UI	UI	V	Hz

The simulator main loop

```
for (simtime=STARTTIME; simtime<=STOPTIME; simtime+=stepsize) {
    update();       /* update nodes each tstep */
    if (simtime-SAVETIME >= savestep*points_plotted) {
        output();
        points_plotted++;
    }
    /* swap pointers to avoid copying data arrays */
    temp = nodeold;
    nodeold = node;
    node = nodenew;
    nodenew = temp;
}
```



The update() routine

```
void update()  /* this routine responsible for updating node[] */
{
    fin(1,FIN,FSTEP,STEPTIME);     /* vo, f, fs, t0 */
    difference(1,8,2);             /* plus, minus, out */
    freq_to_phase(2,3);            /* in, out */
    sing(11,PHIFREQ,180.0*PHIDEV); /* phase modulation input */
    difference(3,11,4);            /* in+, in-, output */
    sample(4,6,UTIME,VPHI,0.0);    /* in, out, utime, swing, err */
    rcfilter(6,7,TAU1);            /* in, out, tau */
    vco(7,8,FVCO,FDEL);            /* in, out, nom, del */
}
```

- notice similiarity to SPICE deck (numbered nodes)
- input “deck” parsing done by C-compiler
- user must assign nodes manually

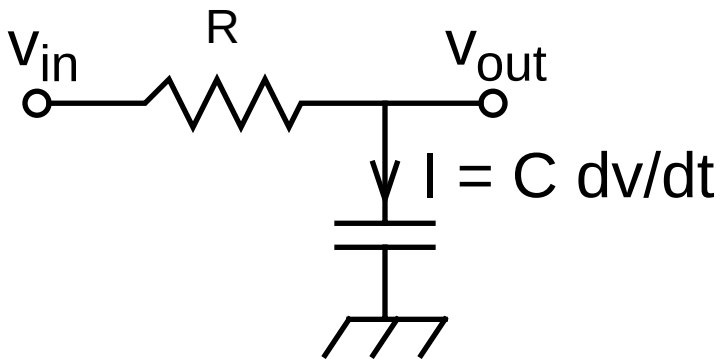
difference() and sine generator code

```
void difference(plus, minus, out)  /* output node = plus - minus */
int plus, minus, out;
{
    nodenew[out] = node[plus] - node[minus];
}
```

```
void sing(out, freq, ampl)  /* a sinusoidal voltage source */
int out;
double freq,ampl;
{
        nodenew[out] = ampl*sin(2.0*M_PI*simtime*freq);
}
```

RC-filter implementation

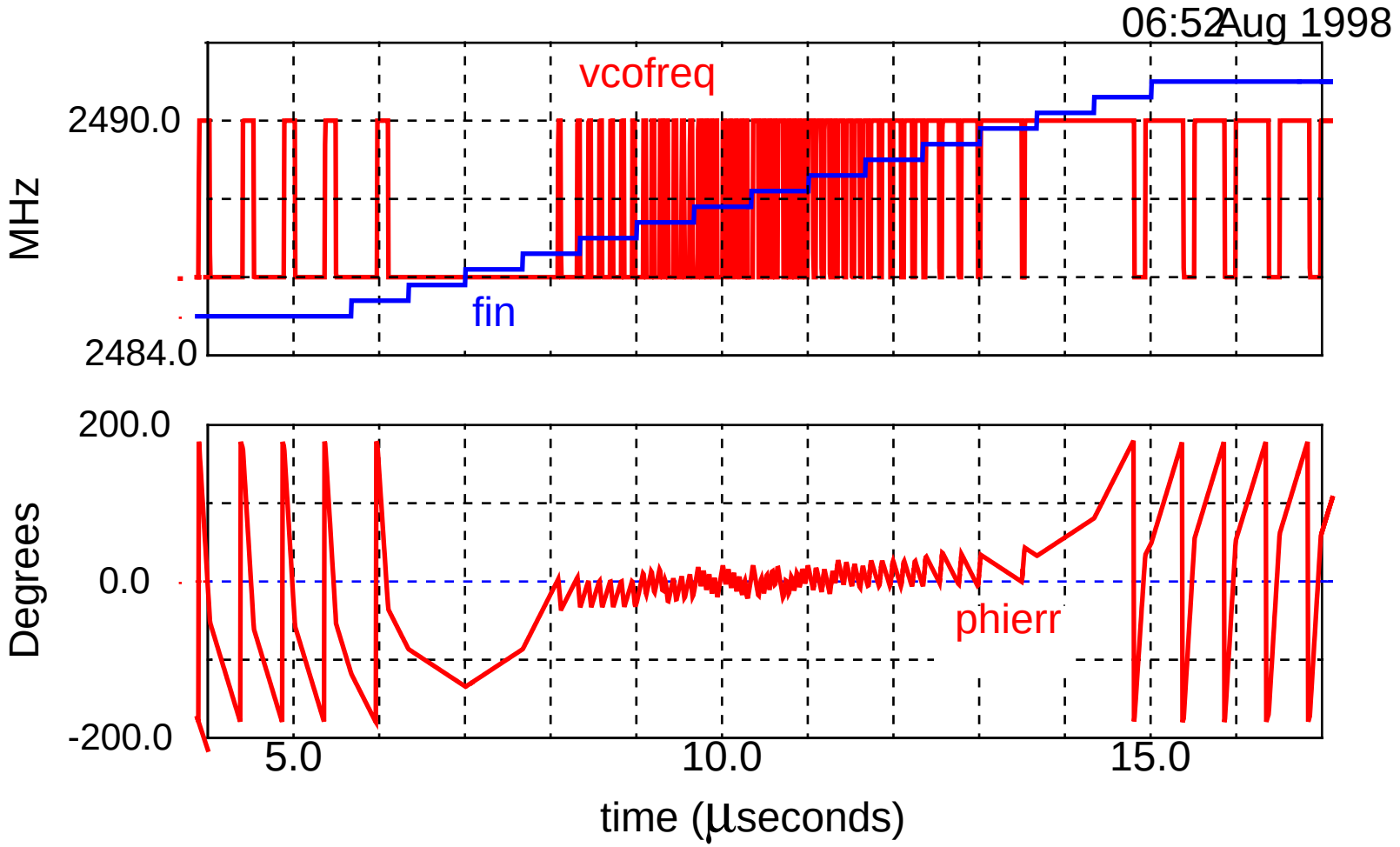
```
void rcfilter(in, out, tau)   /* a single pole rc filter */
int in, out;
double tau;
{
    double temp1, temp2;

    /* Implements discrete diff. eqn:
       Vout = Vin - (tau * dVout/dt)
       where dVout = nodenew[out]-node[out] */

    temp1 = node[in] + tau*(node[out])/stepsize;
    temp2 = 1 + tau/stepsize;
    nodenew[out] = (temp1/temp2);
}
```



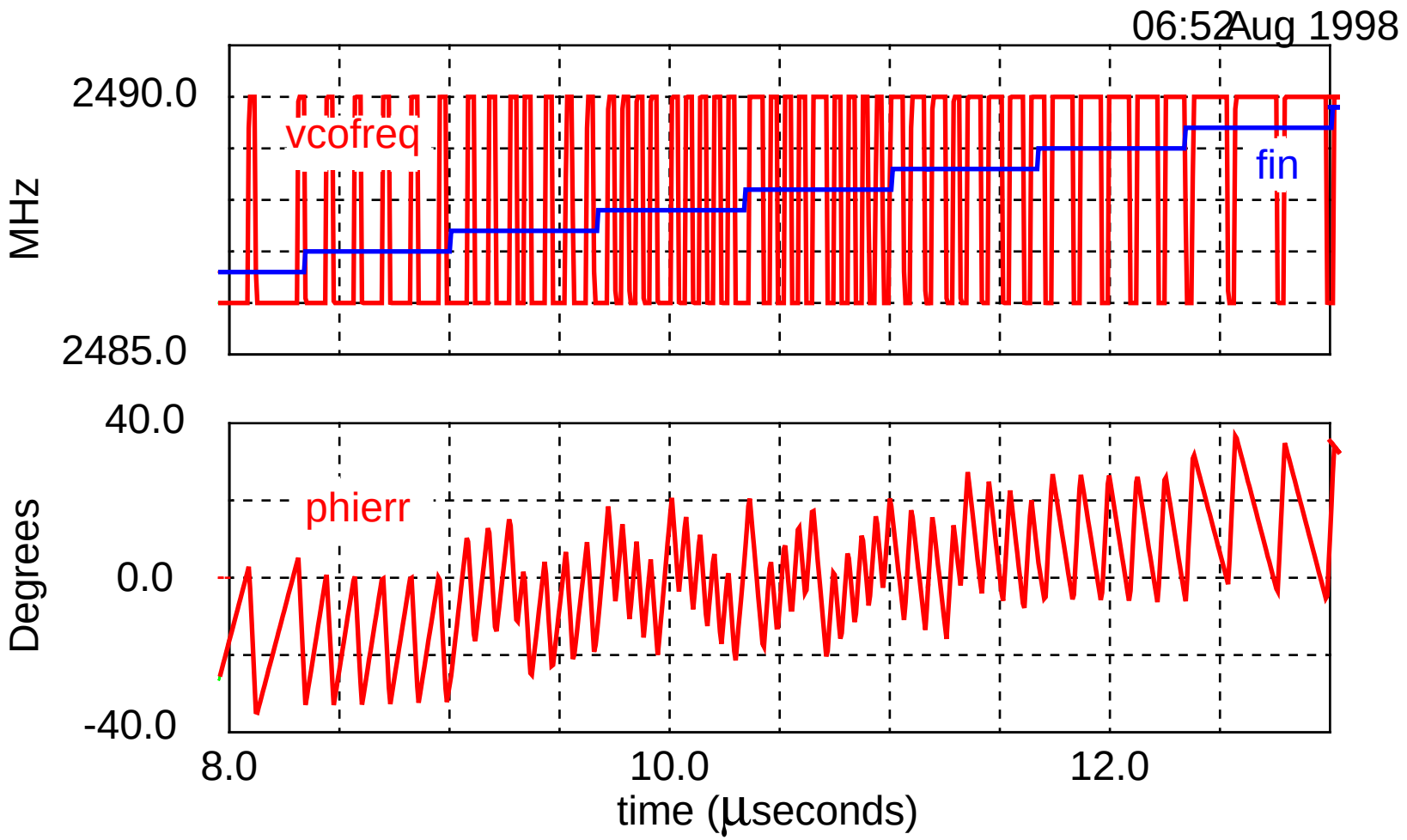
The freq_to_phase() block

```
void freq_to_phase(in, out)   /* performs true integral of input */
int in, out;                  /* scaled by factor of 360. This */
                              /* gives output of 1 volt/degree */
{
    double chunk;   /* new integrated portion of signal */

    chunk = (180.0 * (nodeold[in] + node[in]) * stepsize);
    nodenew[out] = node[out] + chunk;

    # now wrap it into the range of -180 to +180 degrees
    if (nodenew[out] >  180)
        nodenew[out] = nodenew[out]-360;
    if (nodenew[out] < -180)
        nodenew[out] = nodenew[out]+360;
}
```

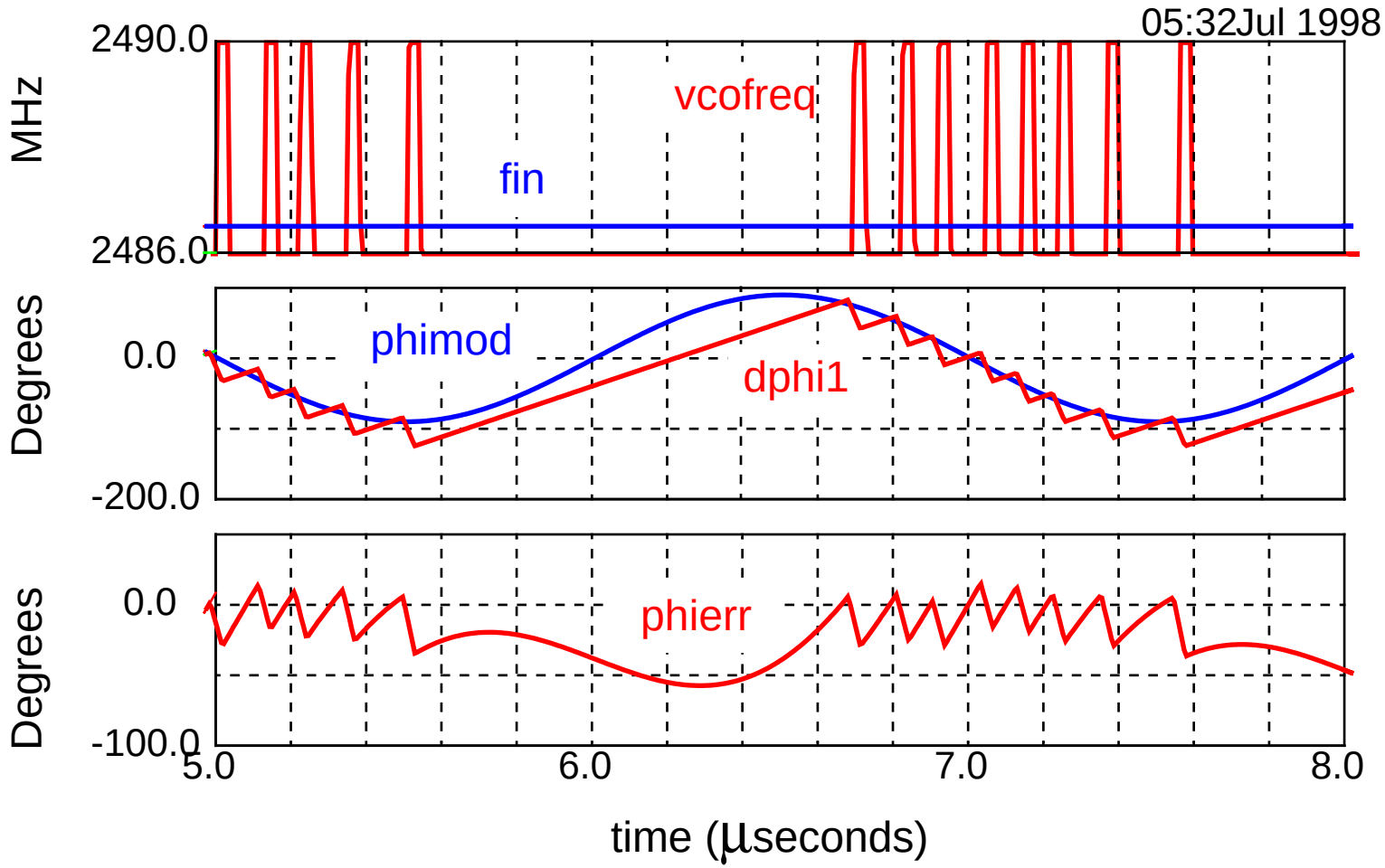
Lock Range for 1st-order loop



1st-order loop: locked region



1st-order loop: slew-rate limiting



Summary of 1st-order loop

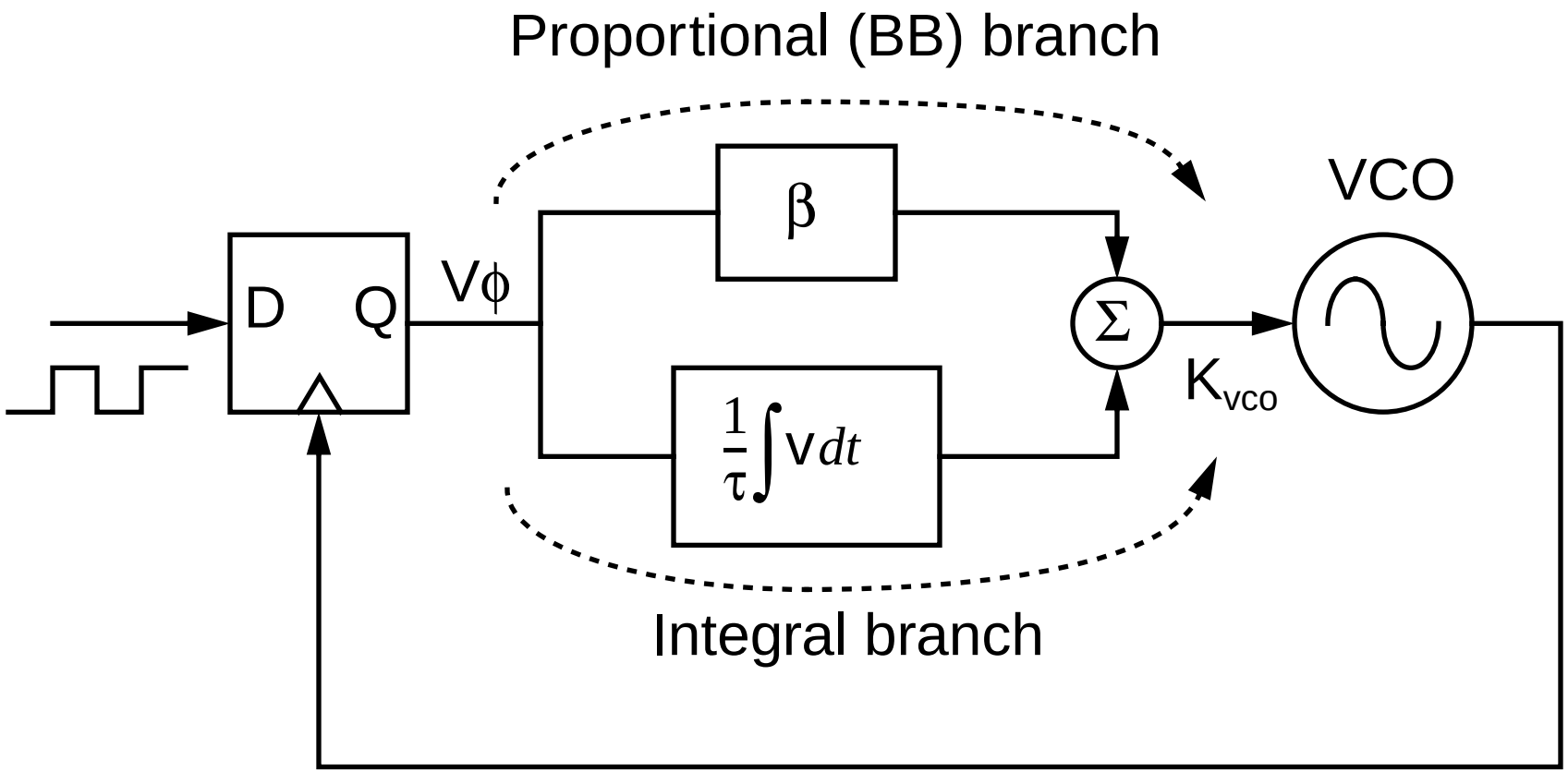
- Lock range: $(f_{nom} + f_{bb}) < f_c < (f_{nom} - f_{bb})$.
- Jitter (peak to peak): $J_{pp} \approx 2 \cdot 360 \cdot t_{update} \cdot f_{bb}$.
- Maximum amplitude of phase modulation at frequency f_{mod} before onset of slew-rate limiting:
- If locked, then the duty cycle C, must result in the average loop frequency being equal to the input frequency f_c,

  $$f_c = f_{nom} + \Delta f = C(f_{nom} + f_{bb}) + (1 - C)(f_{nom} - f_{bb})$$
- Phase detector average duty cycle C, given by $\left(\frac{1}{2} + \frac{\Delta f}{(2 \cdot f_{bb})}\right)$ (proportional to Δf).

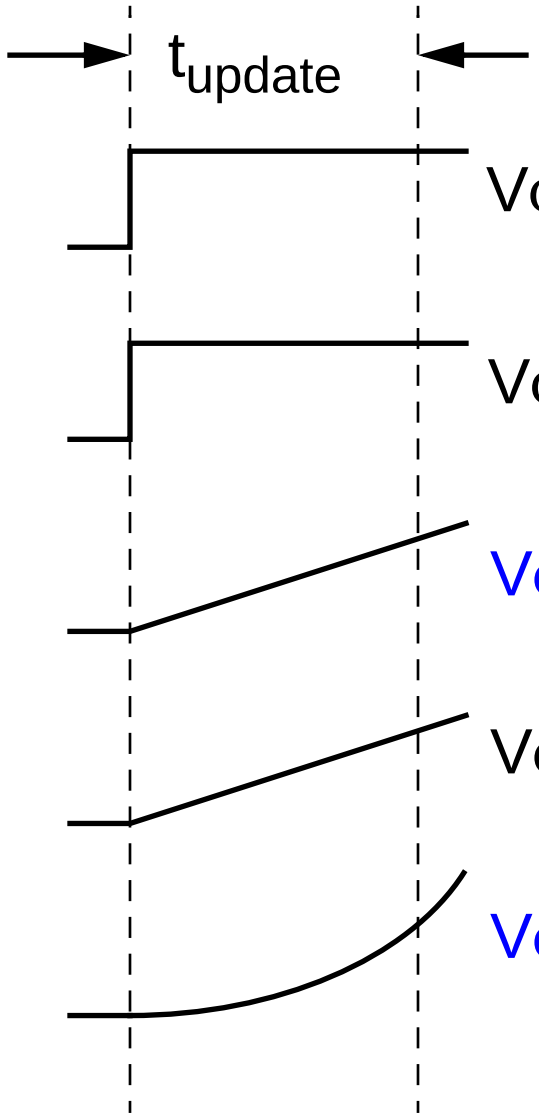
Observations

- Jitter generation, Lock range, and Jitter tolerance are all inconveniently controlled by one parameter, f_{bb}.
- Phase detector average duty-cycle is proportional to frequency error.
- Strategy: Use the average duty cycle to control loop center frequency. This decouples the lock range from jitter tolerance/generation giving more design freedom.

2nd-order BB loop



2nd-order loop step response



$V\phi$ pd output

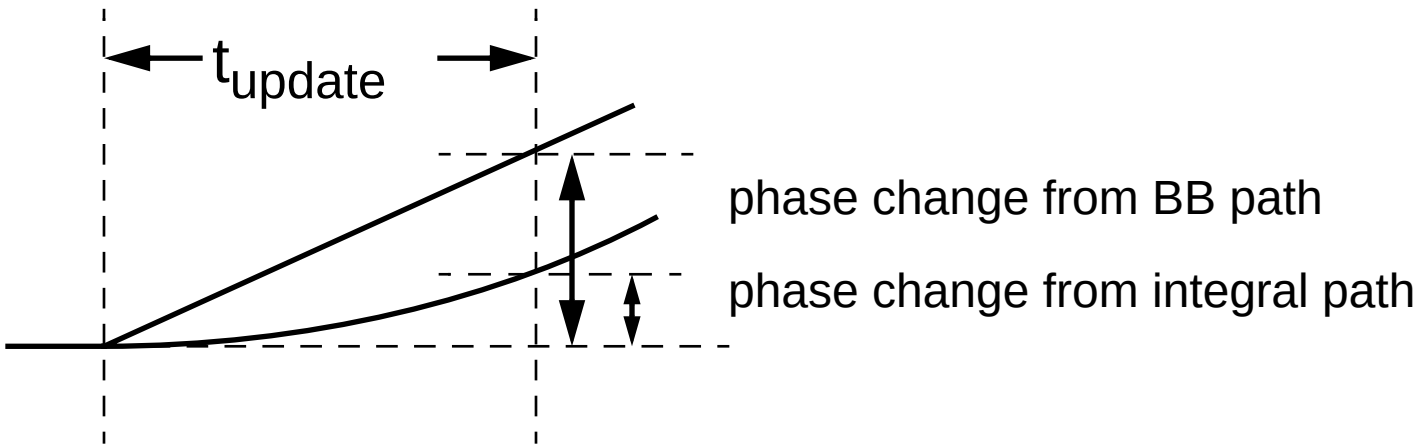
$V\phi\beta K_v$ BB frequency change

$V\phi\beta K_v t$ BB phase phase change

$V\phi K_v t/\tau$ Integrator path frequency change

$V\phi K_v t^2/2\tau$ Integrator path phase change

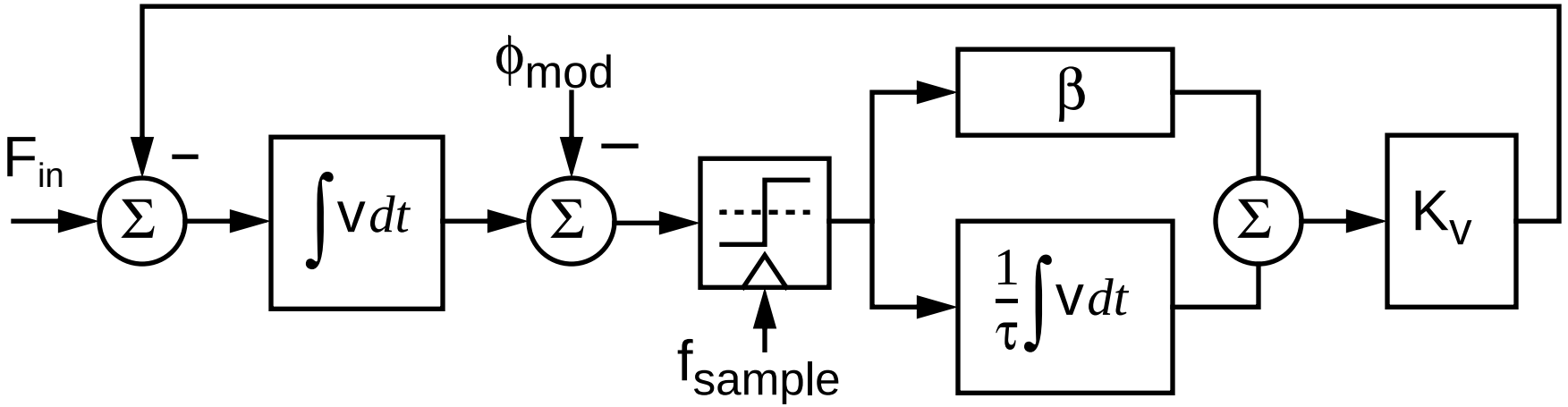
Stability Factor ξ

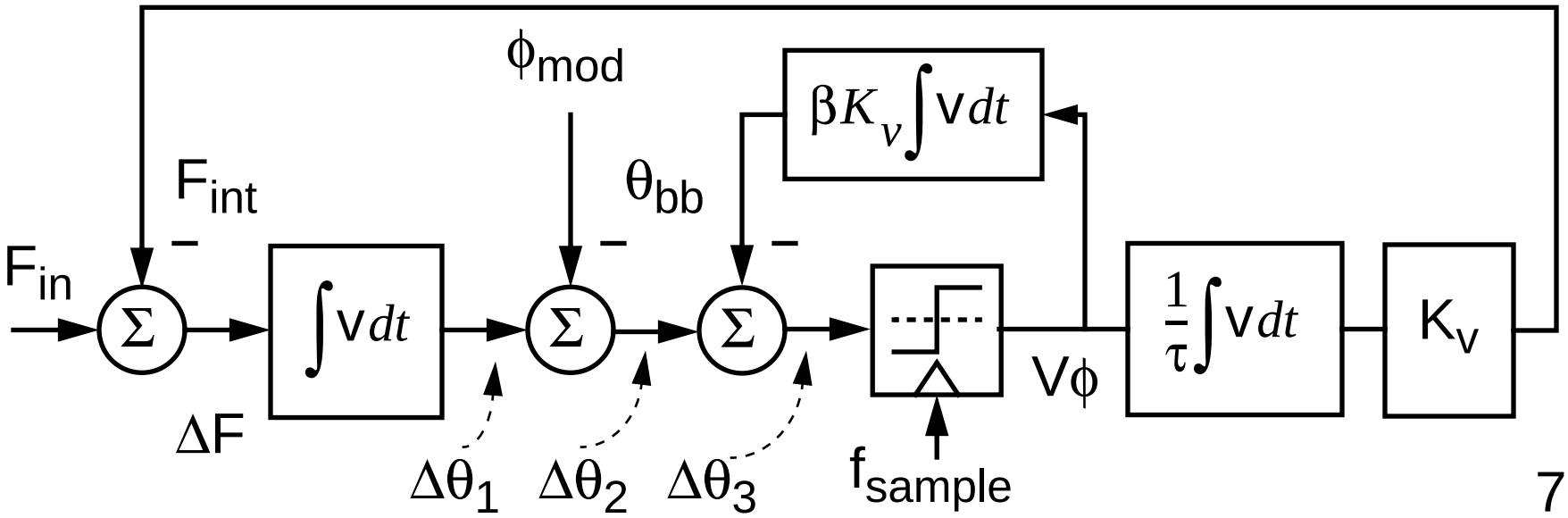


To quantify the relative independance of the two feedback loops, take ratio of phase change from BB path to the phase change of the integral path:

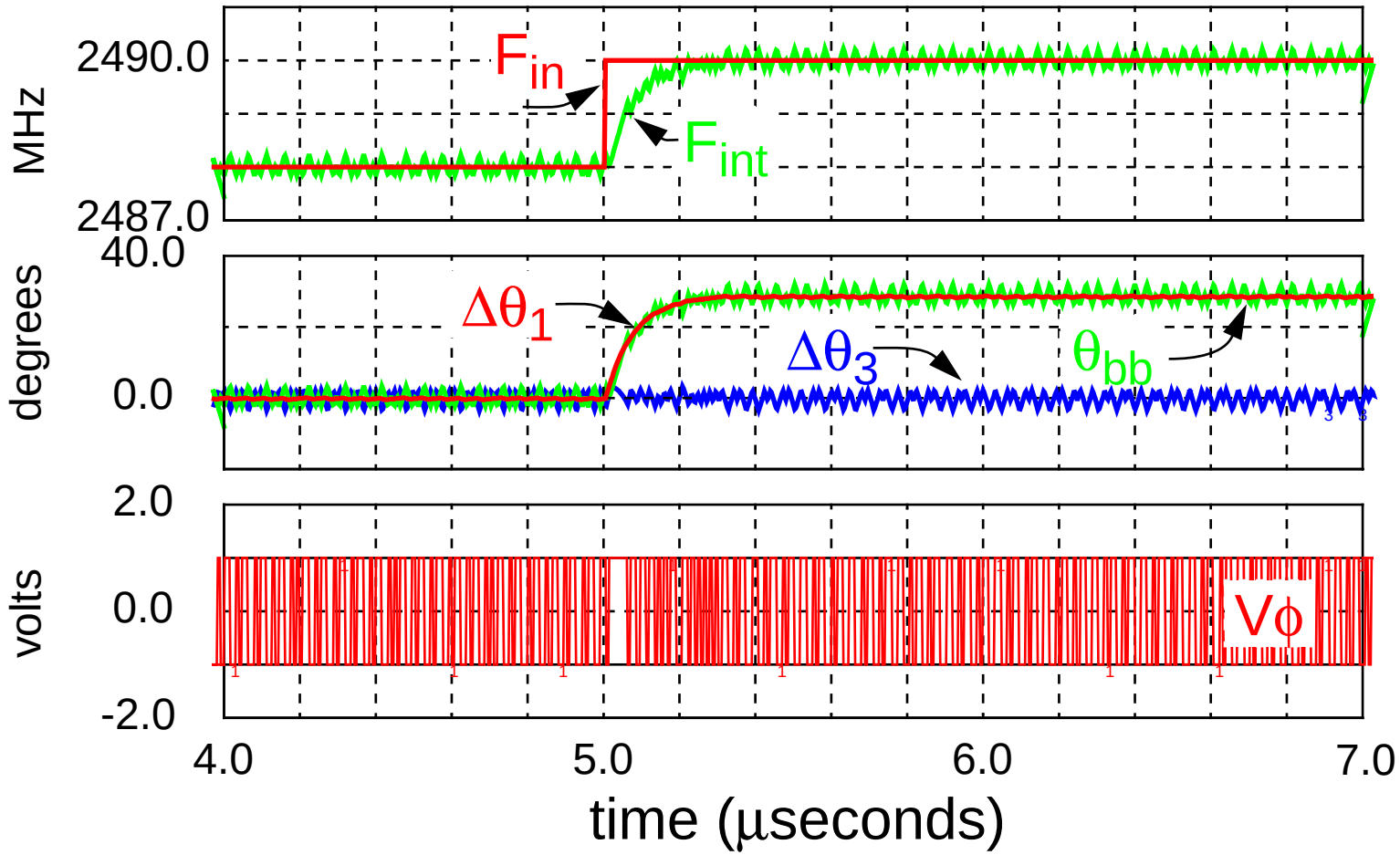
$$\xi \equiv \frac{\Delta\theta_{bb}}{\Delta\theta_{int}} = \frac{\beta V_\phi K_v t}{V_\phi K_v t^2/(2\tau)} = \frac{2\beta\tau}{t_{update}}$$

structural evolution of 2nd-order loop

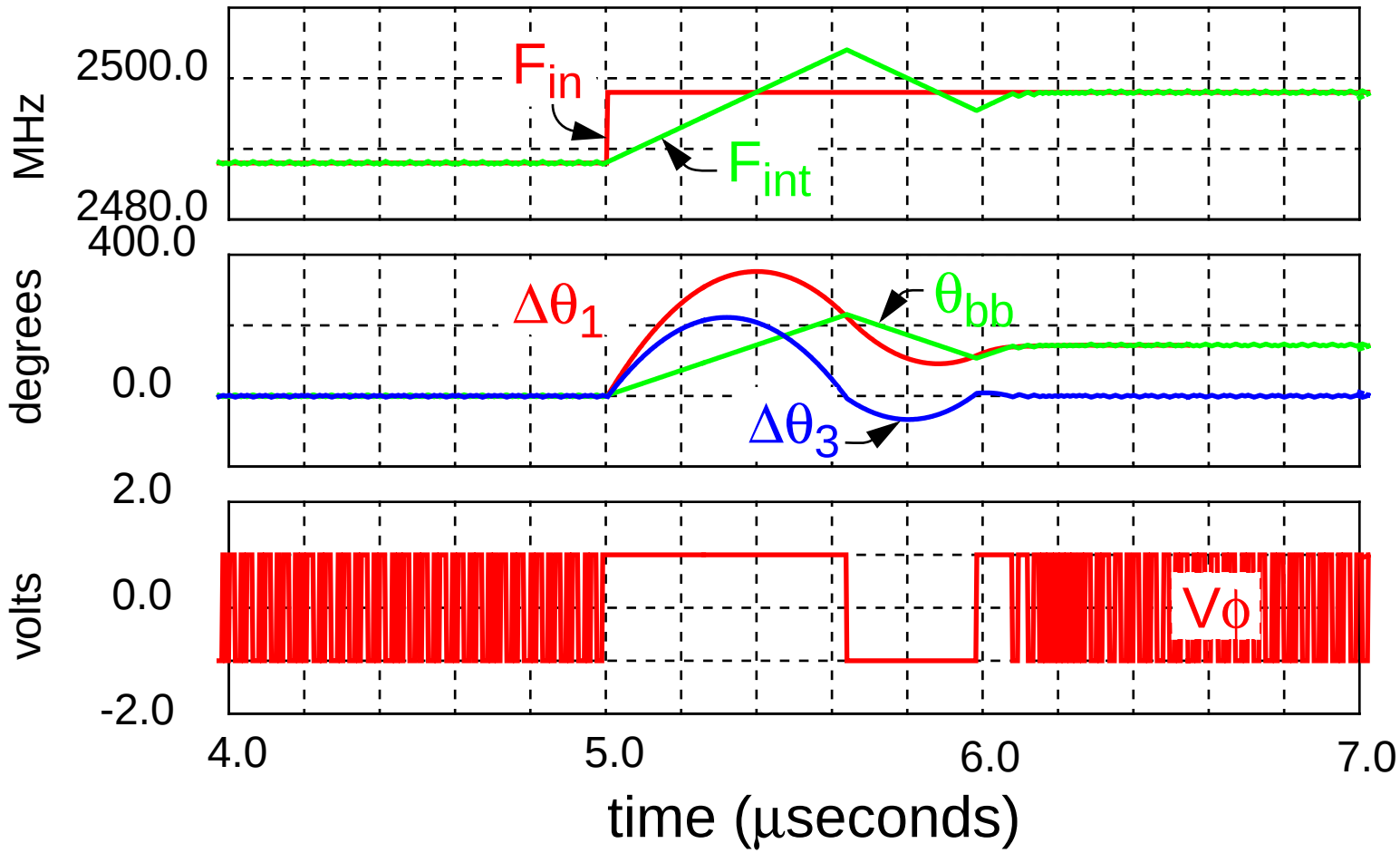




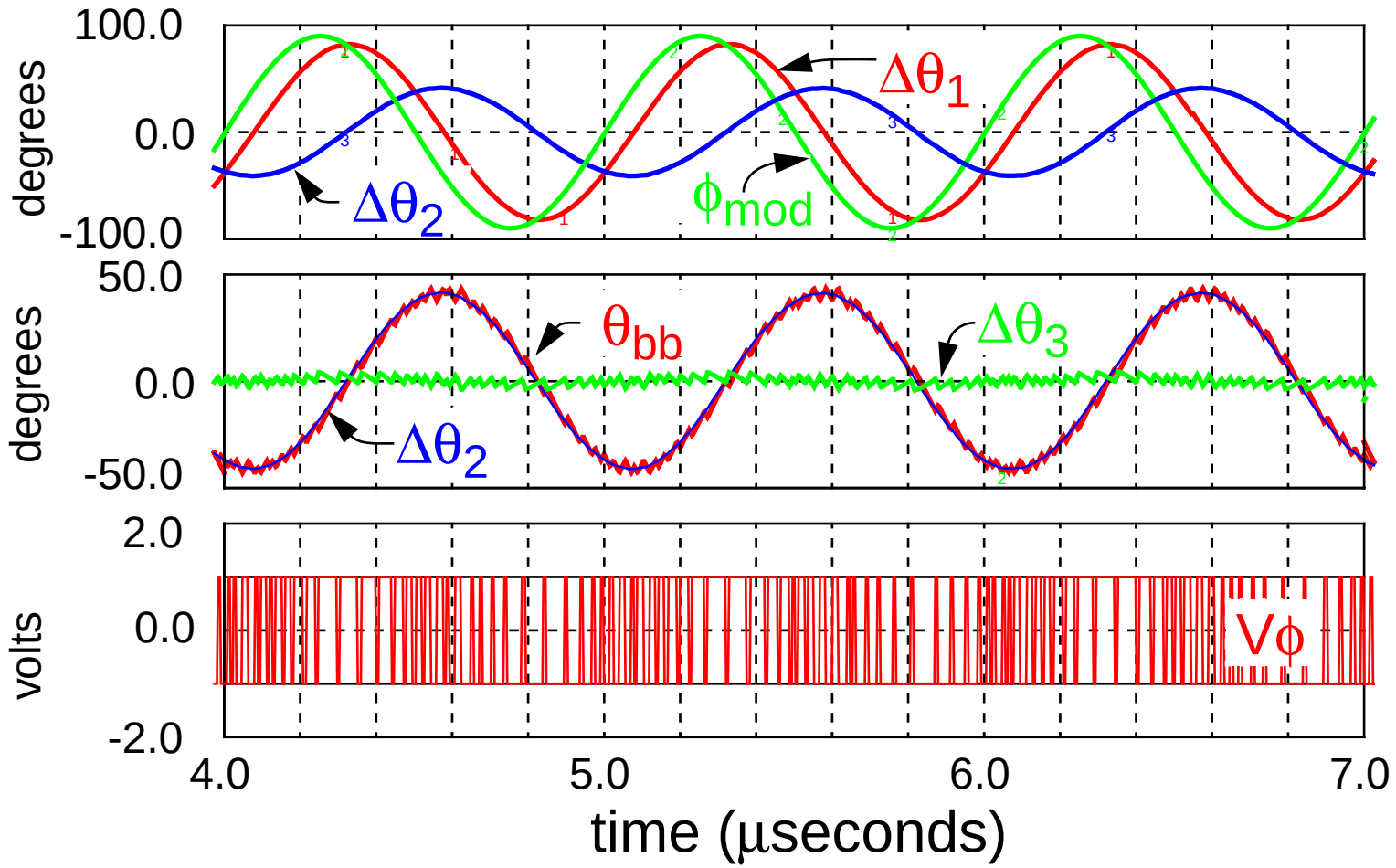
2nd-order loop: small step in F



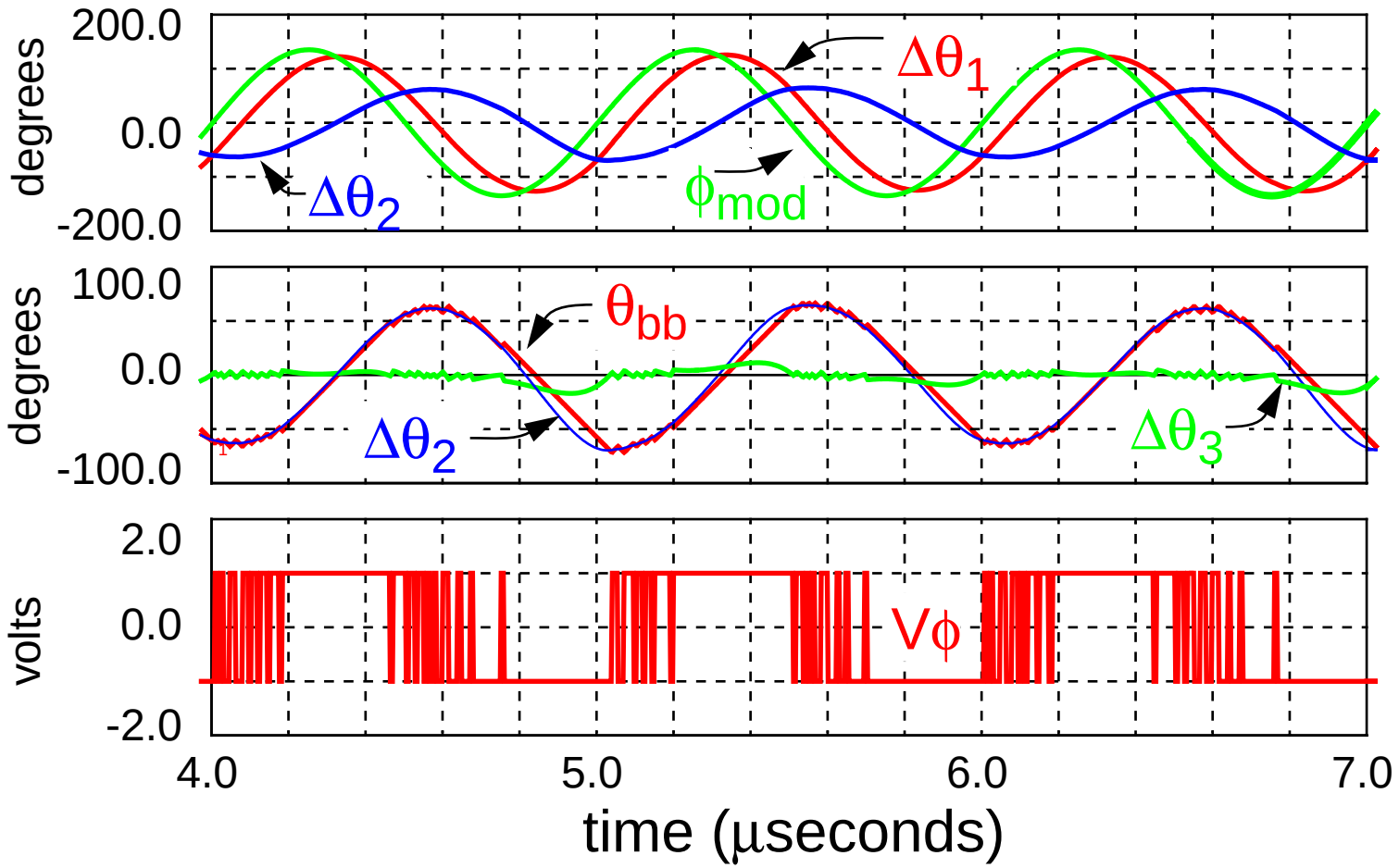
2nd-order loop: large step in F



2nd-order loop: phase jitter tracking

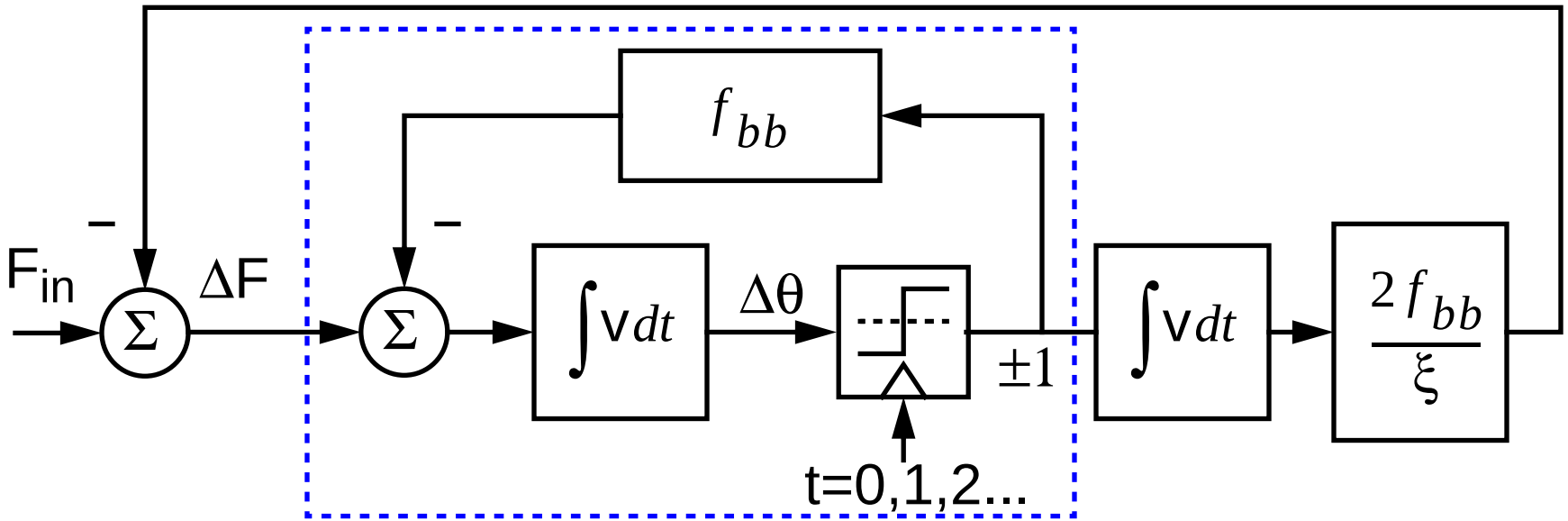


2nd-order loop: slope overload

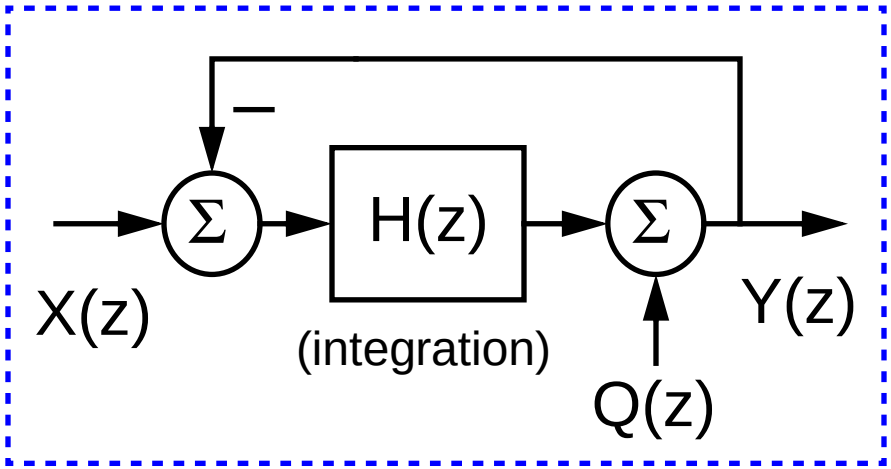


normalized ΔΣ form of 2nd-order loop

- pull integrators through the summing node
- normalize update interval to 1
- let $\beta K_v V\phi = f_{bb}$
- substitute in definition for ξ



$\Delta\Sigma$ linear system analogy for bb-loop

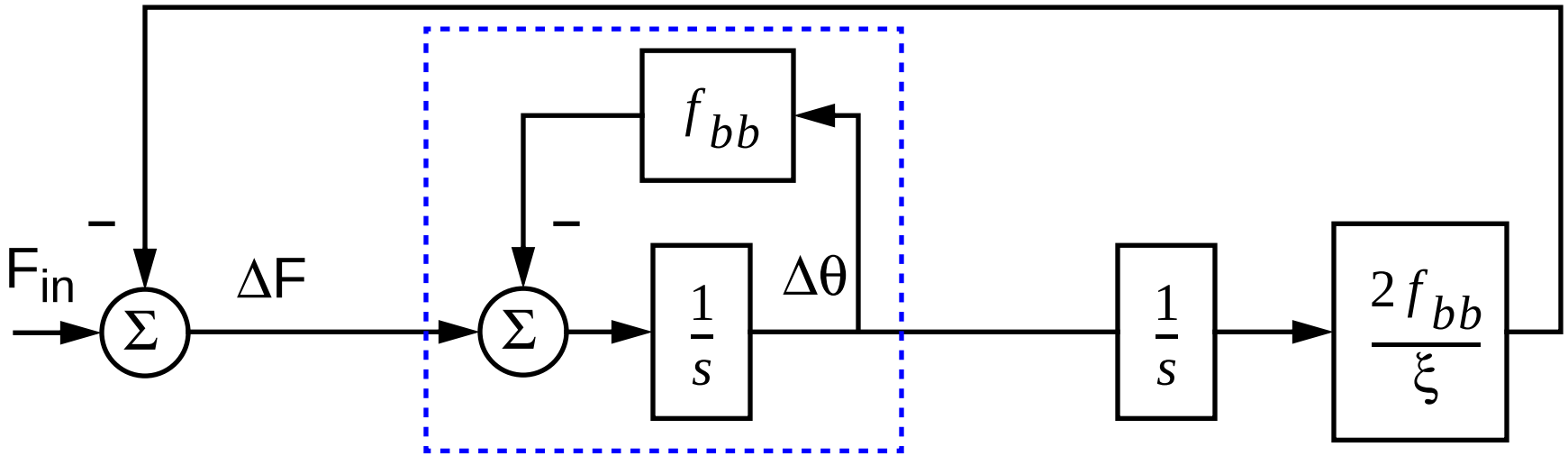


[Hau91b]

[Gal95]

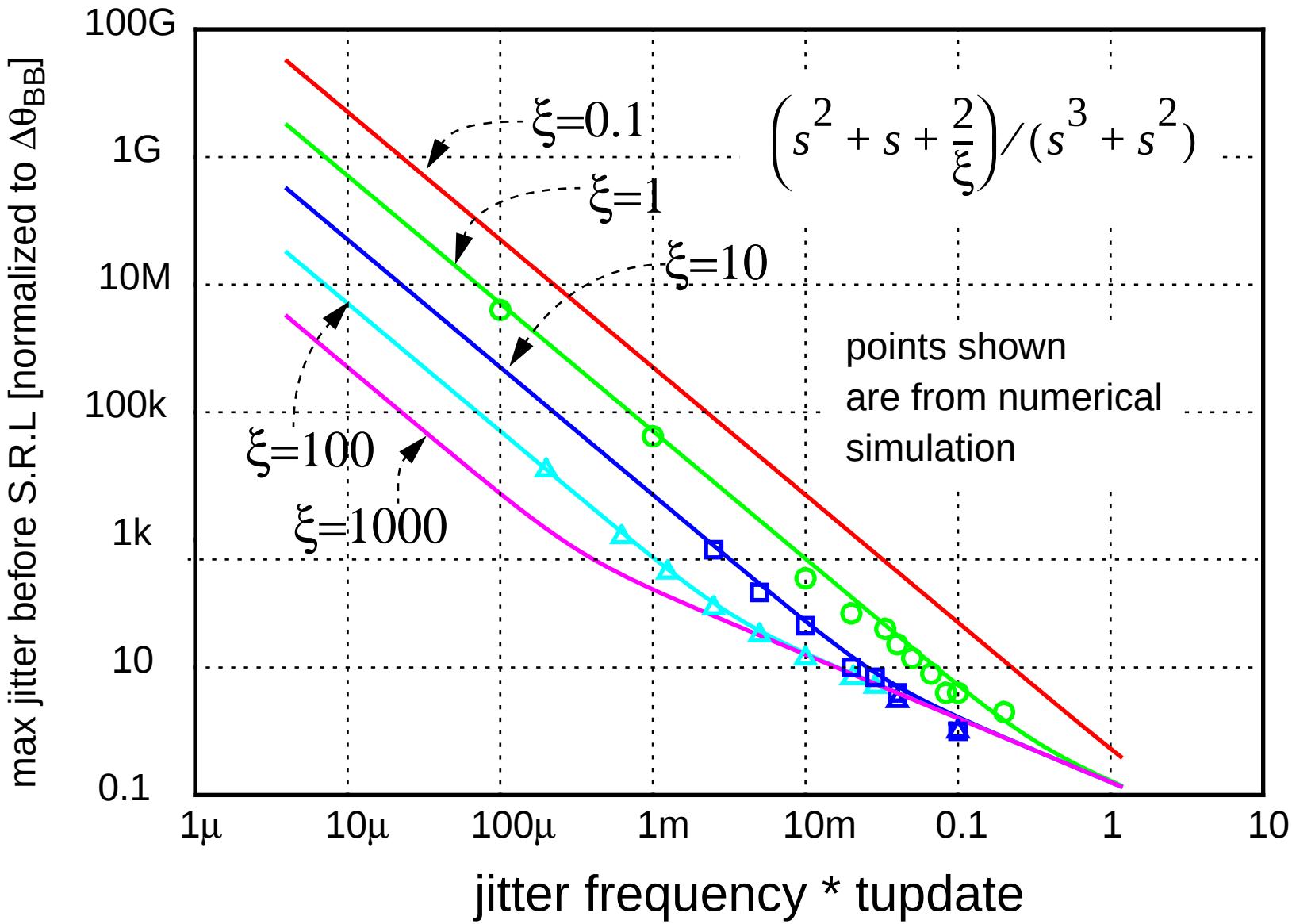
$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Q(z)$$

solve for slope overload



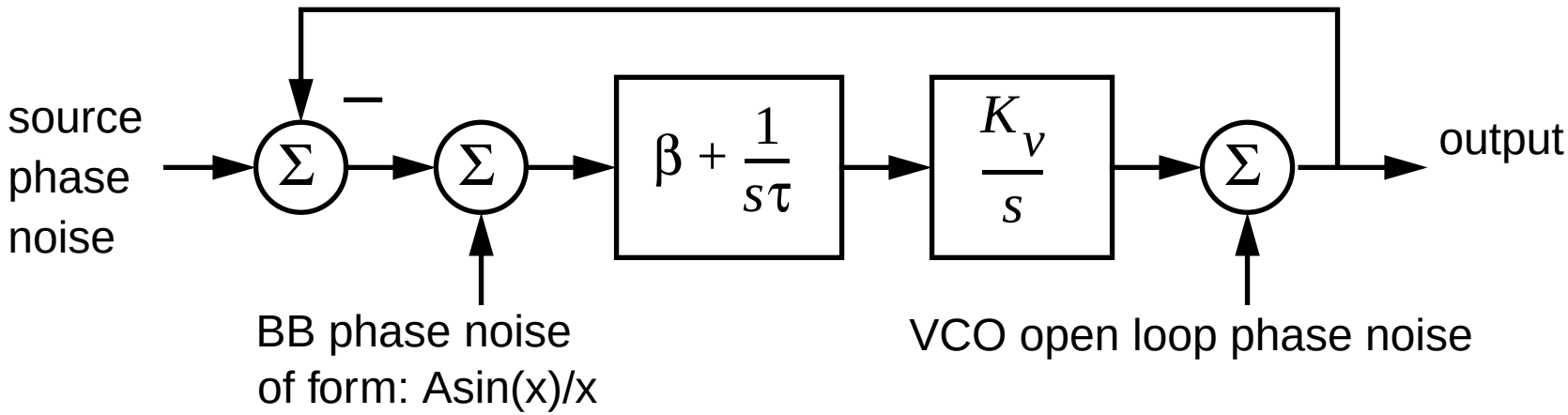
- Slew rate limiting occurs when $\Delta F > f_{bb}$
- Maximum input phase modulation in UI, normalized to $\Delta\theta_{bb}$ is $\left(s^2 + s + \frac{2}{\xi}\right) / (s^3 + s^2)$.

slope overload limit vs ξ



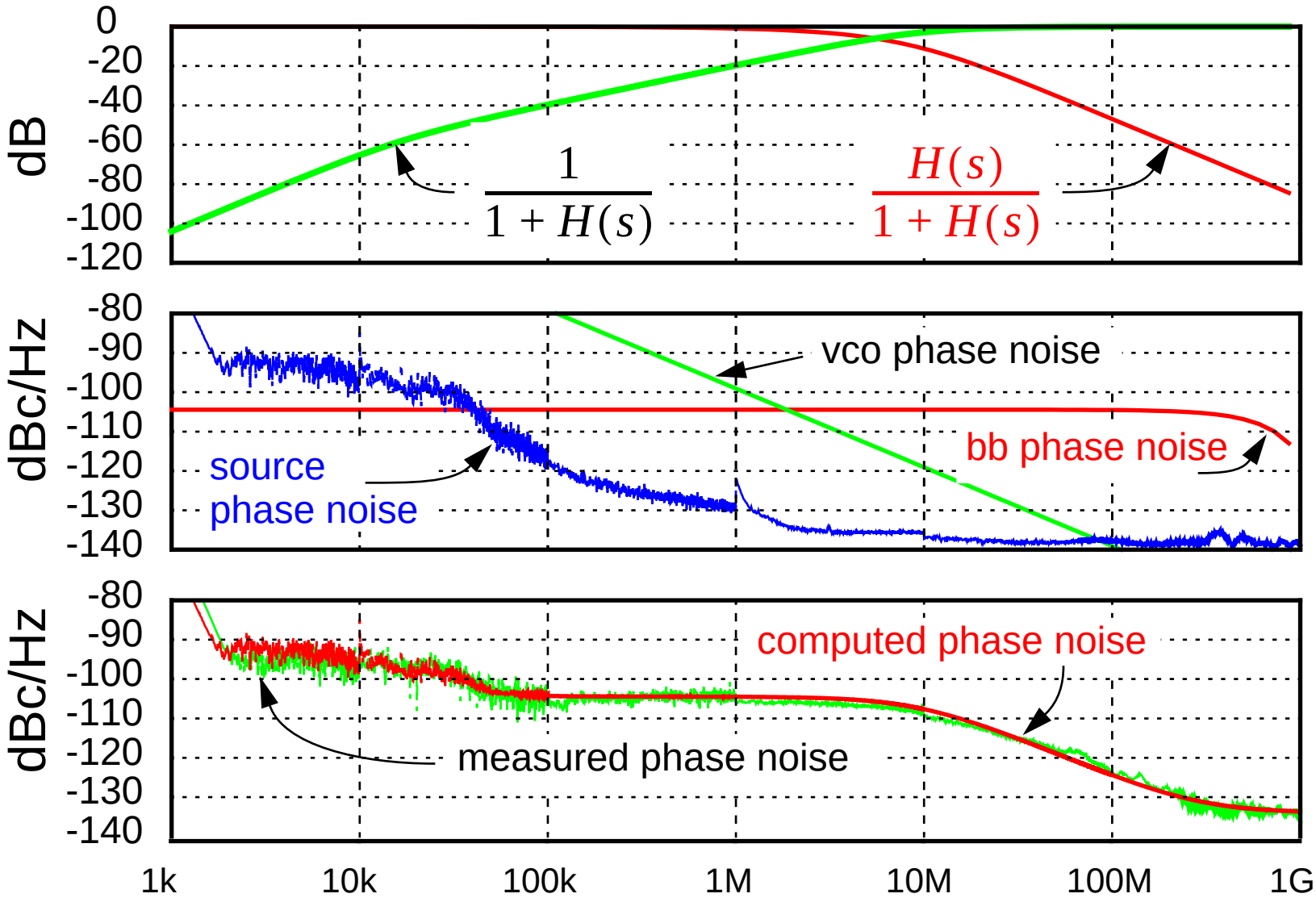
jitter generation in frequency-domain

- $\Delta\Sigma$ approximation justifies replacing BB phase detector with a noise source.
- Combine total loop phase noise by combining each phase noise source in RMS fashion.



$$H(s) = \frac{K_v}{s}\left(\beta + \frac{1}{s\tau}\right)$$

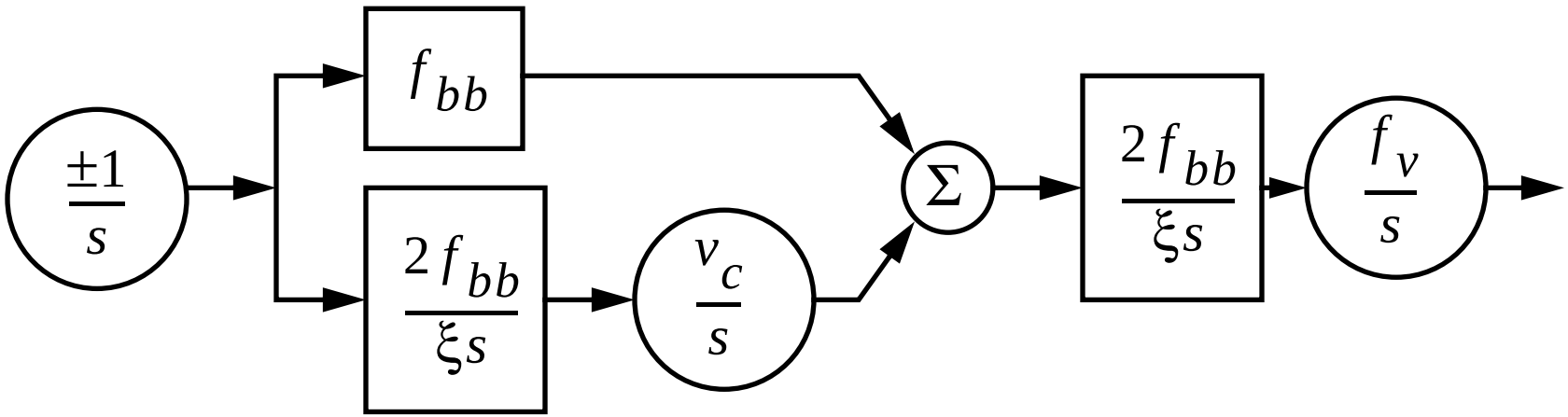
example jitter generation calculation



see [WSY97]: fvco=2.488 GHz, fbb = 6 MHz, ξ=32000, tupdate=400ps.

The ultimate in simulator speed

- Compute precise transient response of system at discrete update times with Laplace transforms.

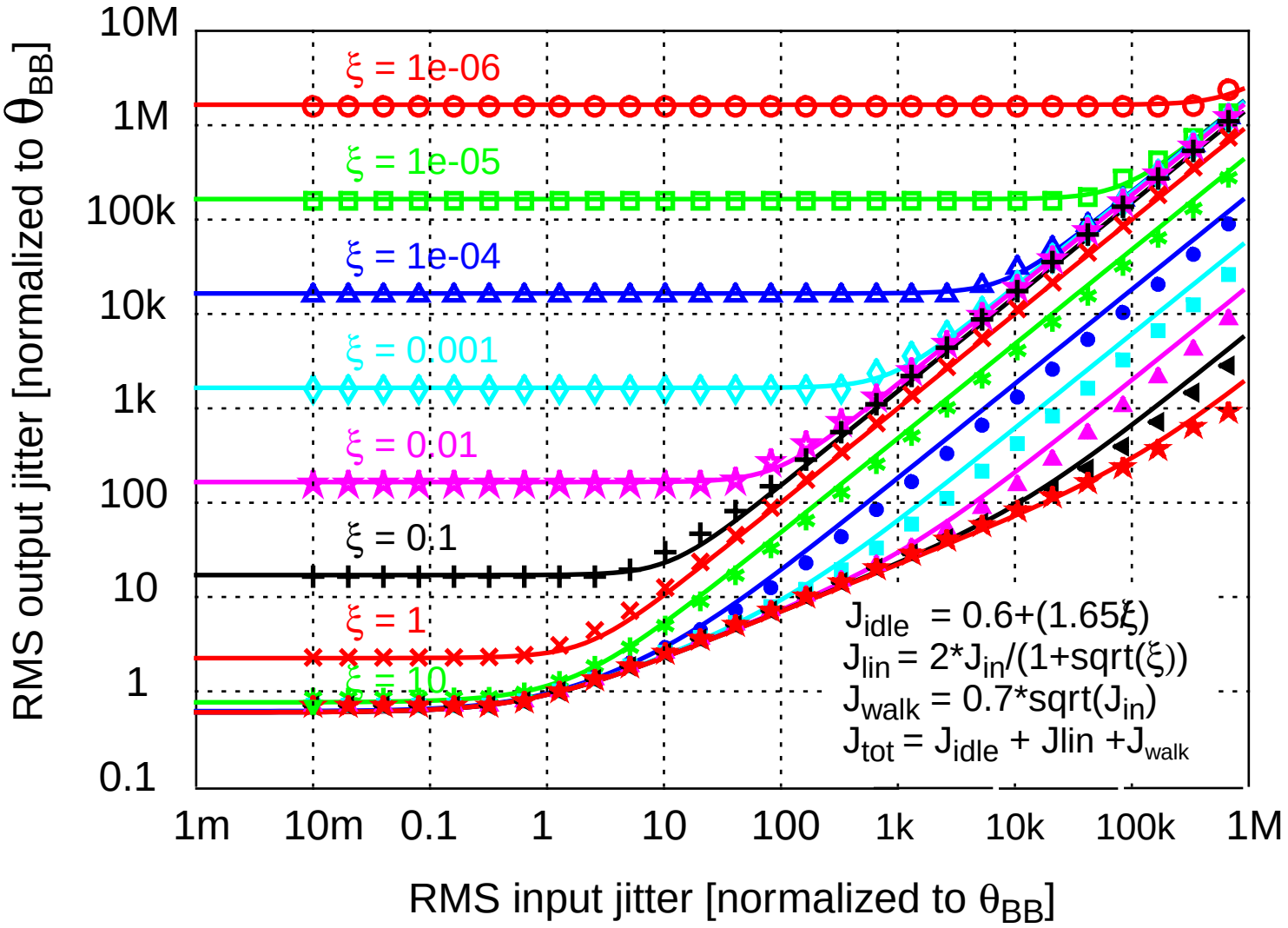


$$\Phi(t+1) = \Phi(t) \pm bb + 2\frac{bb}{\xi}\sum_{0}^{t}(earlylate) \pm \frac{bb}{\xi}$$

simulator core loop

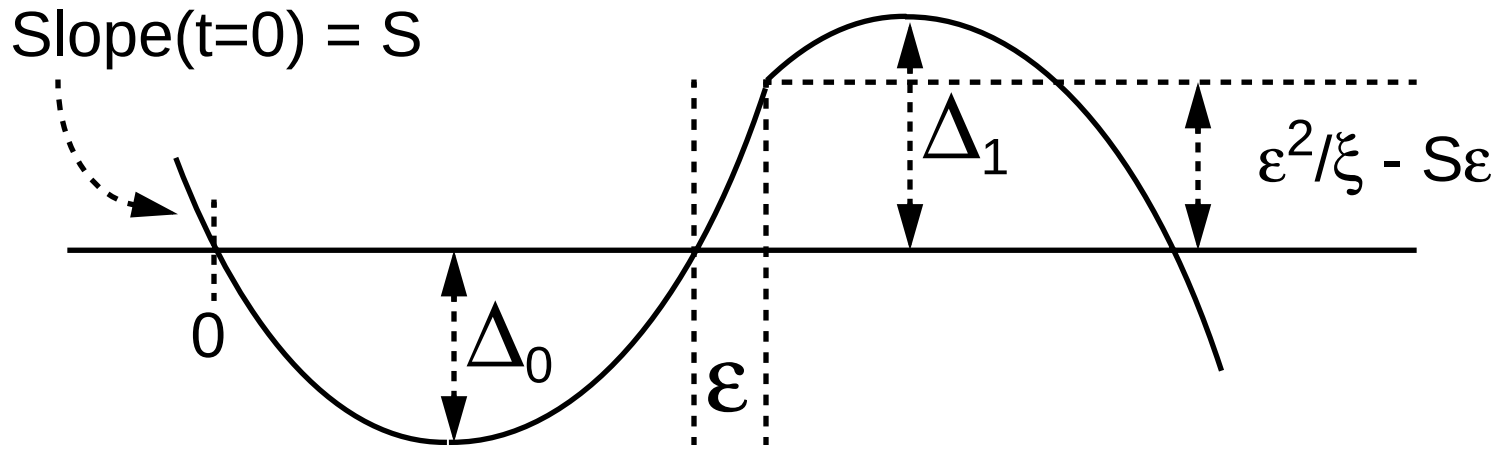
```
for (cycle=1; cycle<=numpoints; cycle++) {

      data_phase = gauss()*jitter;

      vco_phase += direction*bangbang;
      vco_phase += 2.0*loop_filter*bangbang/psi;
      vco_phase += direction*bangbang/psi;

      printf("%d %g\n", cycle, vco_phase);  fflush(stdout);

      direction = (vco_phase >= data_phase) ? (-1) : (1);
      loop_filter += direction;
}
```

gaussian jitter generation & gain vs ξ



(non-tristated loop , $p_{transition}$ = 100% , 10^8 timesteps simulated per point)

Stability with run-length & latency

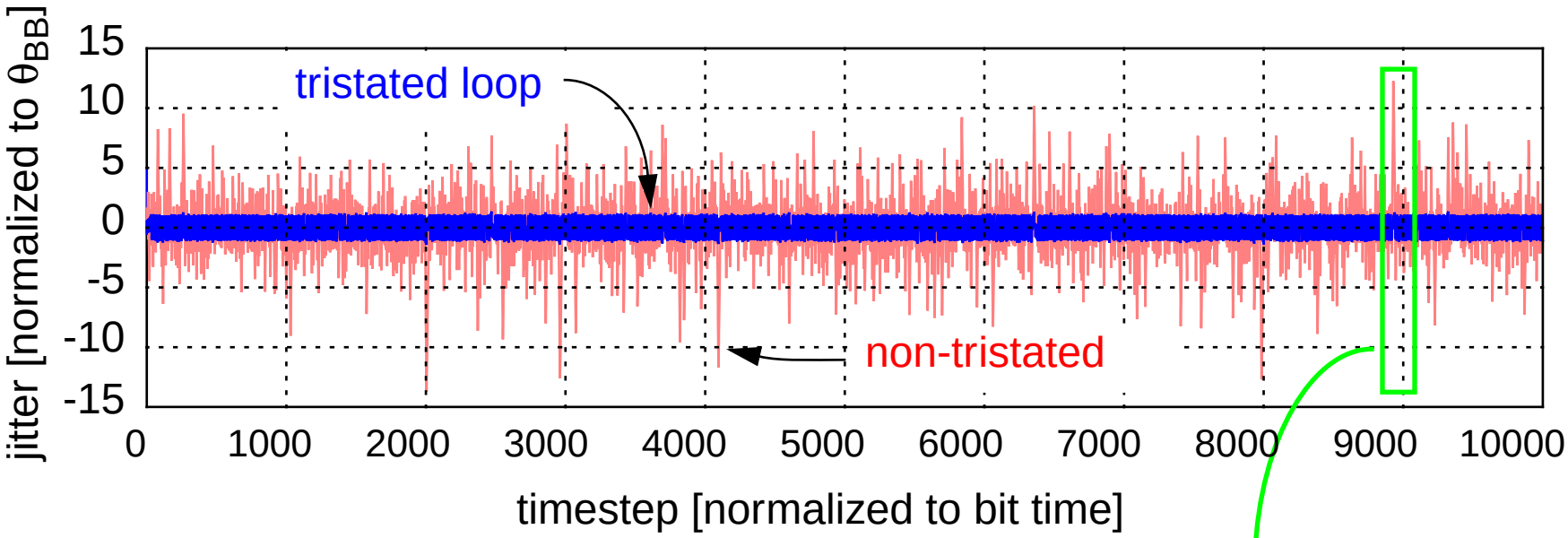


For bounded convergence and stable operation, the overshoot Δ_1 must be less than or equal to the undershoot Δ_0. This condition is guaranteed if

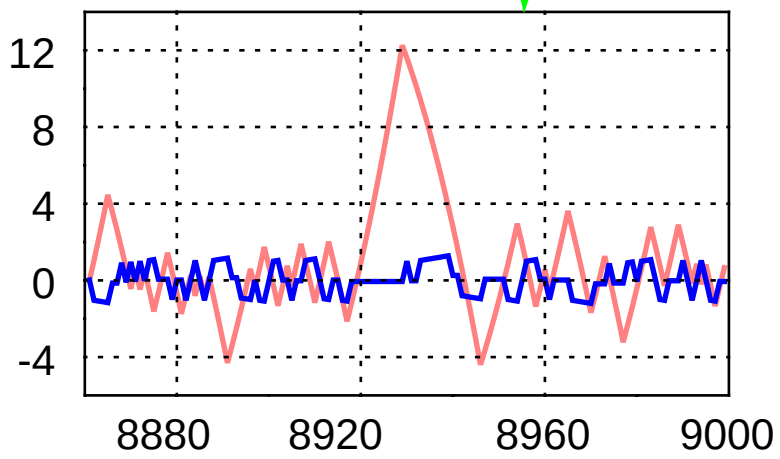
$$\xi > 2\varepsilon$$

(ε is the loop update latency normalized to t_{update})

Effect of BB/charge-pump tristating



- tristating doesn't change vco frequency when no transition in the data.
- Untristated loop has peak jitter *run-length* times worse than tristated loop



(simulated with ξ=100, $p_{transition}$ = 50%)

Public Domain Tools

Linux (a free UNIX clone for INTEL x86 platforms) - Excellent platform for creative circuit design and simulation. See www.cheapbytes.com for a $1.95 distribution CD.

- Homepage: http://www.linux.org/
- Documentation: http://sunsite.unc.edu/mdw/LDP
- Scientific Apps: http://SAL.KachinaTech.COM/index.shtml
    - ACS Circuit simulator
    - EOS Electronic Object Simulator
    - Berkeley SPICE 3f5 (bsim3 models)
    - SCEPTRE

Summary

A lot of complexity for a “simple” system...

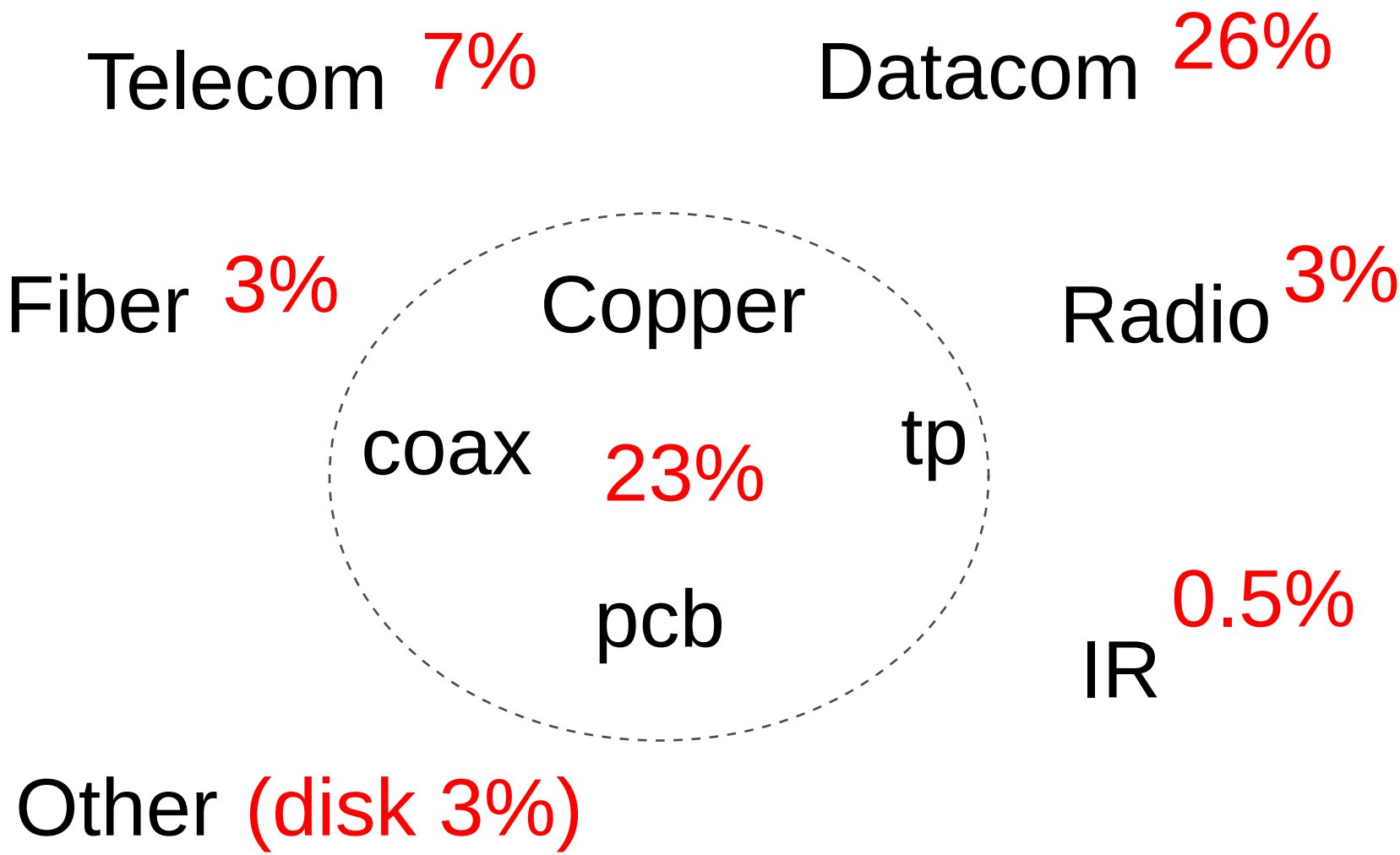
It’s more of an art than a science

After understanding:

- the components,
- the block diagrams,
- the problems and the attempted solutions,
- and the unique needs for your application,

Then it’s time to have fun!

CDR Application Space



numbers estimated from ~250 attendees at February 1997 ISSCC CDR tutorial

CDR Design Checklist

RCW 01/15/97, updated 9/18/98

1) Eye Margin

- how much noise can be added to the input signal while maintaining target BER? (voltage margin)
- How far can clock phase alignment be varied while maintaining target BER? (phase margin)
- how much does the static phase error vary versus frequency, temperature and process variation?
- Is input amplifier gain, noise and offset sufficient?

2) Jitter Characteristics

- what is the jitter generation? (VCO phase noise, etc)
- what is the jitter transfer function? (peaking and bandwidth)
- what is the jitter tracking tolerance versus frequency?

3) Pattern Dependency

- how do long runlengths affect system performance?
- is bandwidth sufficient for individual isolated bit pulses?

- are there other problematic data patterns? (resonances)
- does PLL bandwidth, jitter, and stability change versus transition density?

4) Acquisition Time

- what is the initial, power-on lock time?
- what is the phase-lock aquisition time when input source is changed?

5) How is precision achieved?

- are external capacitors, inductors needed?
- does the CDR need an external reference frequency?
- are laser-trimming or highly precise IC processes required?

6) Input/output impedance

- Is S11/S22 (input/output impedance) maintained across the frequency band?
- are reflections large enough to lead to eye closure and pattern dependency?
- is >15 dB return loss maintained across the band?

7) Power Supply

- does the CDR create power supply noise?
- how sensitive is the CDR to supply noise?
- Is the VCO self-modulated through its own supply noise? (can be “deadly”)

- what is the total static power dissipation?
- what is the die temperature under worse case conditions?

8) False lock susceptibility

- can false lock occur with particular data patterns?
- are false lock conditions be detected and eliminated?
- does the phase detector have VCO frequency leakage that can cause injection locking?
- can the VCO run faster than the phase/frequency detector can operate? (another “killer”)
- have all latchup/deadly embrace conditions been considered and eliminated?

References

[Ale75] Alexander, J. D. H., Clock Recovery from Random Binary Signals, *Electronics Letters 11*, 22 (30th October 1975), 541-542. {binary quantized phase detector}.

[AFD87] Andrews, G. E., D. C. Farley, S. H. Dravitz, A. W. Schelling, P. C. Davis and L. G. McAfee, A 300Mb/s Clock Recovery and Data Retiming System, *ISSCC Digest of Technical Papers*, 1987, 188-189. {SAW Filter Clock Recovery with emphasis on phase alignment problem}.

[Arm83] Armitage, C. B., SAW Filter Retiming in the AT&T 432 Mb/s Lightwave Regenerator, *Conference Proceedings: AT&T Bell Labs., Holmdel, NJ, USA*, September 3-6, 1984, 102-103. {matches tempco of SAW to tempco of electronics.}.

[Baa86] Baack, C., Optical Wide Band Transmission Systems, *CRC Press Inc.*, 1986. {example of PLL for clock recovery}.

[Buc92] Buchwald et al., A., A 6GHz Integrated Phase-Locked Loop using AlGaAs/GaAs Heterojunction Bipolar Transistors, *ISSCC Digest of Technical Papers*, 1992, 98,99,253. {Frequency multiplying ring oscillator}.

[Byr63] Byrne et al., C. J., Systematic Jitter in Chain of Digital Regenerators, *The Bell System Technical Journal*, November 1963, 2679. {clock extraction by filtering}.

[CCI90] CCITT, Digital Line systems based on the synchronous digital hierarchy for use on optical fiber cables, *CCITT G.958*, 1990. {SONET Payload test patterns regenerator scrambling}.

[Car56] Carter, R. O., Low-Disparity Binary Coding System, *Electronics Letters 1*, 3 (May, 1956), 67-68. {conditional inversion data encoding disparity}.

[Cho92] Chona, F. M. R., Draft Standard, SONET inter-office and intra-office line jitter re., *T1X1.3*, May 11, 1992. {Standards SONET jitter}.

[Con84] Connor et al., P. O., A Monolithic Multigigabit/Second DCFL GaAs Decision Circuit, *IEEE Electron Device Letters EDL-5*, 7 (July 1984), 226-227. {GaAs Fet decision circuit example}.

[Cor79] Cordell et al., R. R., A 50MHz Phase and Frequency Locked Loop, *IEEE Journal of Solid State Circuits SC-14*, 6 (December 1979), 1003-1009. {quadricorrellator phase detector, Tunable LC Oscillator}.

[DR78] D'Andrea, N. A. and F. Russo, A Binary Quantized Digital Phase Locked Loop: A Graphical Analysis, *IEEE Transactions on Communications COM-26*, 9 (September 1978), 1355-1364. {Analysis of BB loop}.

[DeV91] DeVito et al., L., A 52 MHz and 155MHz Clock-Recovery PLL, *ISSCC Digest of Technical Papers*, February 13-15, 1991, 142, 143, 306. {multivibrator example, Negative resistor chargepump, rotational freq.det.}.

[Den88] Den Dulk, R. C., Digital Fast Acquisition Method for Phase-Lock Loops, *Electronics Letters 24*, 17 (18th August 1988), 1079-1080. {2 order of magnitude locking speed-up with fancy slip detector & charge pump}.

[EnA87] Enam, S. K. and A. A. Abidi, Decision and clock Recovery Circuits for Gigahertz Optical Fiber Receivers in Silicon NMOS, *Journal of Lightwave Technology LT-5*, 3 (March 1987), 367-372. {MOS tunable monolithic ring oscillator example - Some clever circuit ideas for gigabit rates}.

[EnA92] Enam, S. K. and A. A. Abidi, MOS Decision and Clock Recovery Circuits for Gb/s Optical-Fiber Receivers, *ISSCC Digest of Technical Papers*, 1992, 96,97,253. {quadratic phase detector} {MOS decision circuit example}.

[FHH84] Faulkner, D. W., I. Hawker, R. J. Hawkins and A. Stevenson, An Integrated Regenerator for High Speed Optical Fiber Transmission Systems, *IEE Conference Proceedings* (November 30 - December 1, 1983) 8-13. {uses rectifier/SAW combo}.

[FLS63] Feynman, R., R. B. Leighton and M. Sands, *The Feynman Lectures on Physics*, Addison-Wesley Publishing Company, 1963. {Short, simple presentation of timestep analysis for planetary motion}.

[FMW97] Fiedler, A., R. Mactaggart, J. Welch and S. Krishnan, A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis, *ISSCC Digest of Technical Papers 40* (February 6-8 1997), 238,239,464. {transmit pre-emphasis, skin loss equalizer}.

[Gal94] Galton, I., Higher-order Delta-Sigma Frequency-to-Digital Conversion, *Proceedings of IEEE International Symposium on Circuits and Systems* (May 30 - June 2, 1994) 441-444 {Delta-Sigma BB loops phase tracking frequency digitalization PLL}.

[Gal95] Galton, I., Analog-Input Digital Phase-Locked Loops for Precise Frequency and Phase Demodulation, *Transactions on Circuits and Systems-II: Analog and Digital Signal Processing* 42, 10 (October 1995), 621-630. {good discussion of delta-sigma analysis of BB PLL's}.

[Gar79] Gardner, F. M., *Phaselock Techniques, Second Edition*, John Wiley and Sons, Inc., 1979. {example of using exor-gate to generate clock component from NRZ data}.

[Gla85] Glance, B. S., New Phase-Lock Loop Circuit Providing Very Fast Acquistion Time, *IEEE Transactions on Microwave Theory and Techniques MTT-33*, 9 (September 1985), 747-754. {adds non-linear time constant to speed PLL acquisition by 2 orders of mag.}.

[Gri69] Griffiths, J. M., Binary Code Suitable for Line Transmission, *Electronics Letters 5*, 4 (February 20, 1969), 79-81. {5b/6b encoding example}.

[GMP78] Gruber, J., P. Marten, R. Petschacher and P. Russer, Electronic Circuits for High Bit Rate Digital Fiber Optic Communication Systems, *IEEE Transactions on Communications COM-26*, 7 (July 1978), 1088-1098.

[Gup75] Gupta, S. C., Phase-Locked Loops, Proceedings of the IEEE 63, 2 (February 1975), 291-306. {Good systematic outline survey of communication-type PLL's}.

[Hau91a] Hauenschild et al., J., A Silicon Bipolar Decision Circuit Operating up to 15Gb/s, *IEEE Journal of Solid State Circuits 26*, No.11 (November 1991), 1734-1736. {Si bipolar decision circuit example}.

[Hau91b] Hauser, M. W., Principles of Oversampling A/D Conversion, *J. Audio Eng. So. Vol 39*, 1/2 (Jan/February 1991), 3-26. {excellent tutorial on Delta Sigma AD, Oversampling, noiseshaping}.

[HeS88] Hein, J. P. and J. W. Scott, z-Domain Model for Discrete-Time PLL's, *IEEE Transactions on Circuits and Systems 35*, 11 (November 1988), 1393-1400. {good discussion of using z-transforms in PLL analysis}.

[Hog85] Hogge, Jr., C. R., A Self Correcting Clock Recovery Circuit, *IEEE Transactions on Electron Devices ED-32*, 12 (December 1985), 2704-2706. {Original Hogge detector, interesting phase detector idea...}.

[Hor92] Hornak, T., Interface Electronics for Fiber Optic Computer Links, *Intensive Course on Practical Aspects in Analog IC Design*, Lausanne, Switzerland, June 29-July 10, 1992. {Excellent overview of components for serial optical data transmission}.

[Hu93] Hu, T. and P. Gray, A Monolithic 480 Mb/s AGC/Decision/Clock Recovery Circuit in 1.2 um CMOS, *IEEE Journal of Solid State Circuits 28*, 12 (Dec. 1993) 1314-20 {CMOS parallel signal paths multiphase sampling CDR mux}.

[Kas85] Kasper et al., B. L., SAGM Avalanche Photodiode Optical Receiver for 2 Gbit/s and 4 Gbit/s, *Electronic Letters 21*, 21 (10th October 1985), 982-984. {eye diagram}.

[KWG94] Kim, B., T. C. Weigandt and P. R. Gray, PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design, *ISCAS proceedings*, May 30 - June 2, 1994, 31-34. {Excellent and Intuitive discussion of Jitter in Ring Oscillators}.

[Lai90] Lai, B., Decision Circuit Lowers Transmission Bit Error Rates, *Microwaves and RF,* July 1990, 118- 122. {Si bipolar decision circuit example}.

[LaW91] Lai, B. and R. C. Walker, A Monolithic 622Mb/s Clock Extraction Data Retiming Circuit, *ISSCC Digest of Technical Papers 34* (February 13-15, 1991), 144,145. {binary quantized phase detector}.

[Lam93] Lam, V. M. T., Microwave Oscillator Phase Noise Reduction Using Negative Resistance Compensation, *Electronics Letters 29*, 4 (February 18th, 1993), 379-340. {Leeson negative resistance phase noise second harmonic IC}.

[LiC81] Lindsey, W. C. and C. M. Chie, A Survey of Digital Phase-Locked Loops, *Proceeding of the IEEE 69*, 4 (April 1981), 410-431. {Presents a good taxonomy of digital PLLs}.

[Mac87] MacDougall, M. H., *Simulating Computer Systems - Techniques and Tools*, The MIT Press, Cambridge, Massachusetts, 1987. {description and source code for event driven simulator}.

[McG90] McGaughey, J. T., Convert NRZ format to Biphase, *Electronic Design,* April 12, 1990, 86. {biphase example}.

[OFC84] O'Connor, P., P. G. Flahive, W. Clemetson, R. L. Panock, S. H. Wemple, S. C. Shunk and D. P. Takahashi, A Monolithic Multigigabit/Second DCFL GaAs Decision Circuit, *IEEE Electron Device Letters EDL-5*, 7 (July 1984),. {2.4 GHz ED GaAs Mesfet Flip-flop w/ input buffer amp}.

[Ofe89] Ofek, Y., The Conservative Code for Bit Synchronization, *IEEE Transactions on Communications,* 1989. {conserves transition number uses divider for clock recovery}.

[OhT83] Ohta, N. and T. Takada, High Speed GaAs SCFL Monolithic Integrated Decision Circuit for Gb/s Optical Repeaters, *Electronics Letters*, September 1983. {GaAs Decision Circuit}.

[Par89] Park et al., M. S., Novel Regeneration Having Simple Clock Extraction and Automatic Phase Controlled Retiming Circuit, *Electronic Letters 25* (January 1989), 83-84. {clock extraction by filtering}.

[Pet88] Petrovic, R., Low Redundancy Optical Fiber Line Code, *Journal of Optical Communication 9*, 3 (1988), 108-111. {13B/14B code design}.

[RaO91] Ransijn, H. and P. O'Connor, A PLL-Based 2.5-Gb/s GaAs Clock and Data Regenerator IC, *JSSC 26*, 10 (October 1991), 1345-1353. {Rotational frequency detector, Limiting Amp, Jitter Transfer Measurement}.

[Raz96a] B. Razavi, ed., *Monolithic phase-locked loops and clock recovery circuits: theory and design*, IEEE Press, 1996. {A volume of selected reprints with bibliography}.

[Raz96b] Razavi, B., Monolithic Phase-Locked Loops, *ISSCC Tutorial*, San Francisco, CA, February 7, 1996. {Good overview of non-data-driven PLL theory}.

[ReG73] Reddy, C. P. and S. C. Gupta, A Class of All-Digital Phase Locked Loops: Modeling and Analysis, *IEEE Transactions on industrial Electronics and Control Instrumentation IECI-20*, 4 (November 1973), 239-251. {discusses of binary-quantized phase detection}.

[RCF84] Rosenberg, R. L., C. Chamzas and D. A. Fishman, Timing Recovery with SAW Transversal Filters in the Regenerators of Undersea Long-Haul Fiber Transmission Systems, *Journal of Lightwave Technology LT-2*, 6 (December 1984), 917-925. {discusses jitter accumulation}.

[Ros84] Rosenberg et al., R. L., Timing Recovery with SAW Transversal filters in the Regenerators of Undersea Long-haul Fiber Transmission Systems, *IEEE Journal of Lightwave Technology LT-2*, 6 (December 1984), 917-925. {clock extraction by SAW}.

[Ros85] Ross, F. E., An Overview of FDDI: the Fiber Distributed Data Interface, *IEEE Journal on Selected Areas in Communications 7*, 7 (September 1985), 1046, Table 1. {4b/5b encoding example, example of frame synch characters}.

[RHF90] Ross, F. E., J. R. Hamstra and R. L. Fink, FDDI - A LAN among MANs, *ACM Computer Communications Review*, July 1990, 16-31. {4b/5b encoding example}.

[Rou76] Rousseau, M., Block Codes for Optical-Fibre Communication, *Electronics Letters 12*, 18 (2nd September 1976), 478-479. {mBnB code discussion, run length limits, power spectra, 5b6b recommended}.

[RoM77] Roza, E. and P. W. Millenaar, An Experimental 560 MBit/s Repeater with Integrated Circuits, *IEEE Transactions on Communications COM-25*, 9 (September 1977),. {coax-based. good comparison of PLL vs filter-type clock extraction}.

[RuG91] Runge, K. and J. L. Gimlett, 20Gb/s AlGaAs HBT Decision Circuit IC, *Electronics Letters 27*, 25 (5th December 1991), 2376-2378. {GaAs HBT decision circuit example}.

[Run91] Runge et al., K., Silicon Bipolar Integrated Circuits for Multi-Gb/s Optical Communication Systems, *IEEE Journal on Selected Areas in Communications 9*, 5 (June 1991), 640. {Si bipolar decision circuit example}.

[San82] Sandera, L., Improve Datacomm Links by Using Manchester Code, EDN, February 17, 1982, 155-162. {manchester coding example}.

[Shi87] Shin et al., D., Selfcorrecting Clock Recovery Circuit with Improved Jitter Performance, *Electronics Letters 23*, 3 (29th January 1987), 110-111. {Improved Hogge detector}.

[SyA86] Syed, K. E. and A. A. Abidi, Gigahertz Voltage Controlled Oscillator, *Electronics Letters 22* (June 5, 1986), 677-679. {MOS tunable monolithic ring oscillator example}.

[TrV89] Trischitta, P. R. and E. L. Varma, *Jitter in digital transmission systems*, Artech House, Inc., 1989. {good overview of jitter (textbook) ISBN 0-89006-248-X}.

[Wal89] Walker, R. C., Fully Integrated High Speed Voltage Controlled Ring Oscillator, *U.S. Patent 4,884,041*, Granted Nov. 28, 1989. {Si bipolar tunable monolithic ring oscillator example}.

[WHY91] Walker, R. C., T. Hornak, C. Yen, J. Doernberg and K. H. Springer, A 1.5Gb/s Link Interface Chipset for Computer Data Transmission, *IEEE Journal on Selected Areas in Communications 9*, 5 (June 1991), 698-703. {binary quantized phase detector with master transition}.

[WWS92] Walker, R., J. Wu, C. Stout, B. Lai, C. Yen, T. Hornak and P. Petruno, A 2-Chip 1.5Gb/s Bus-Oriented Serial Link Interface, *ISSCC Digest of Technical Papers 35* (February 19-21 1992), 226,227,291. {MT Code, Ring Osc} binary quantized phase detector with master transition}.

[WSY97] Walker, R., C. Stout and C. Yen, A 2.488Gb/s Si-Bipolar Cloc k and Data Recovery IC with Robust Loss of Signal Detection, *ISSCC Digest of Technical Papers 40* (February 6-8 1997), 246,247,466. {training loop, loss of signal detection, bb-loop, ring oscillator}.

[WHK98] Walker, R. C., K. Hsieh, T. A. Knotts and C. Yen, A 10Gb/s Si-Bipolar TX/RX Chipset for Computer Data Transmission, *ISSCC Digest of Technical Papers 41* (February 5-7 1998), 302,303,450. {multi-phase architecture, 8-phase VCO, ft-doubler amplifier, bb-loop}.

[WKG94] Weigandt, T. C., B. Kim and P. R. Gray, Analysis of Timing Jitter in CMOS Ring Oscillators, *ISCAS proceedings, May 30 - June 2, 1994*. {Excellent and Intuitive discussion of Jitter in Ring Oscillators}.

[WiF83] Widmar, A. X. and P. A. Franaszek, A DC Balanced, partitioned-Block 8B/10B Transmission Code, *IBM Journal of Research and Development 27*, 5 (September 1983), 440-451. {8b/10b encoding example - Precursor to Fiber Channel's 8B/10B code}.

[Wu92] Wu, J. and R. C. Walker, A Bipolar 1.5Gb/s Monolithic Phase Locked Loop for Clock and Data Extraction, *VLSI Circuit Symposium*, Seattle, June 3-5, 1992. {positive feedback PLL loop filter}.

[YTY80] Yamada, J., J. Temmyo, S. Yoshikawa and T. Kimura, 1.6 Gbit/s Optical Receiver at 1.3um with SAW Timing Retrieval Circuit, *Electronics Letters*, 1980, 57-58. {basic SAW system, with discussion of power penalty for SAW phase shifts}.

[Yam80] Yamada et al., J., 1.6Gb/s Optical Receiver at 1.3um with SAW Timing Retrieval Circuit, *Electronics Letters 16*, 2 (17th January 1980), 57- 58. {clock extraction by SAW}.

[YFW82] Yen, C., Z. Fazarinc and R. Wheeler, Time-domain skin-effect model for transient analysis of lossy transmission lines., *Proceedings of the IEEE 70*, 7 (July 1982), 750-757. {skin-effect lossy transmission line transient simulation modelling}.

[YKI84] Yoshikai, N., K. Katagiri and T. Ito, mB1C Code and its Performance in an Optical Communication System, *IEEE Transactions on Communications COM-32*, 2 (February 1984). {uses m binary bits + one complementary bit stuffed to break runs}.