A 2.488 Gb/s Si-Bipolar Clock and Data Recovery IC with Robust Loss of Signal Detection

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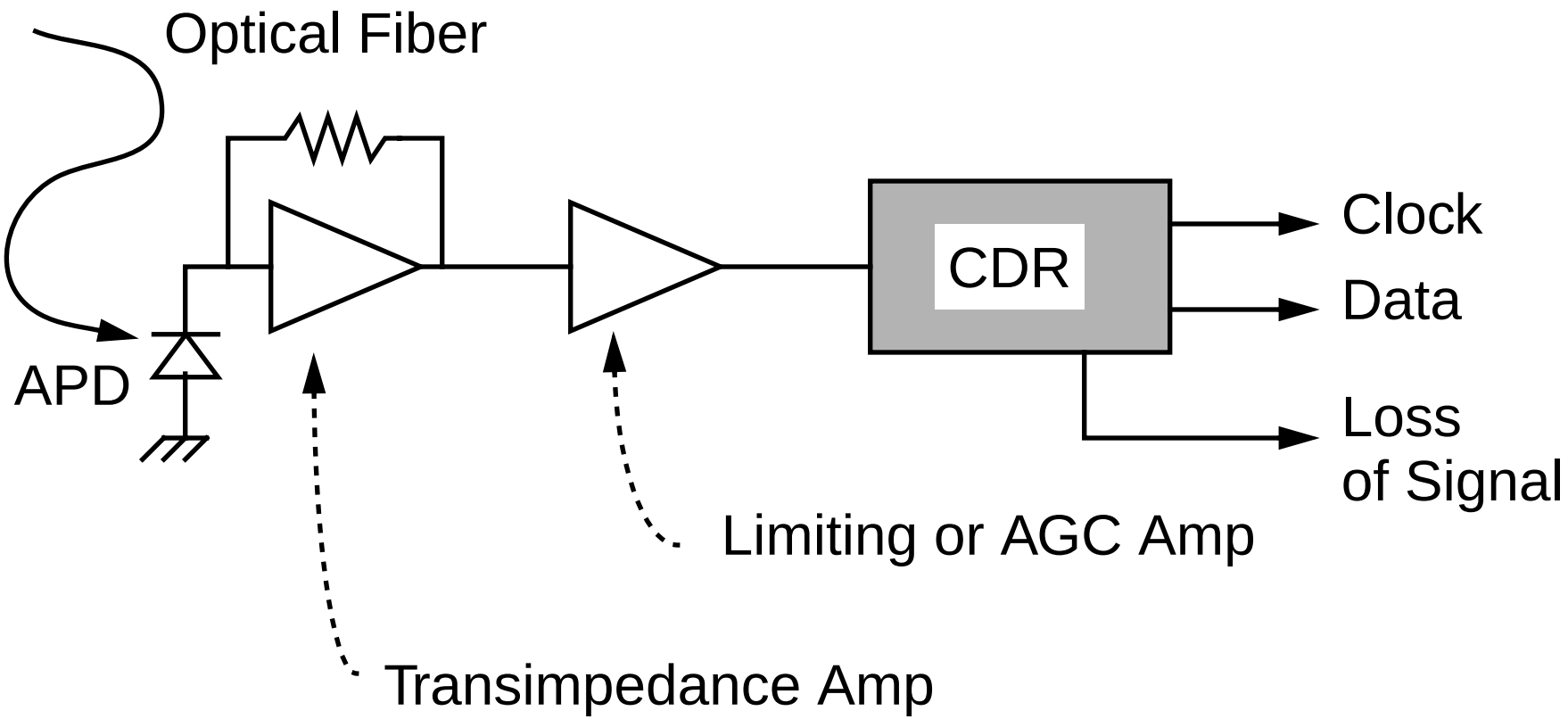
Outline

- System Overview and Design Goals
- Critical Component: VCO
- Chip Architecture
- Need for Loss of Signal (LOS) Function
- Phase, Transition, and Data Lock detector
- LOS circuit
- Measured Results

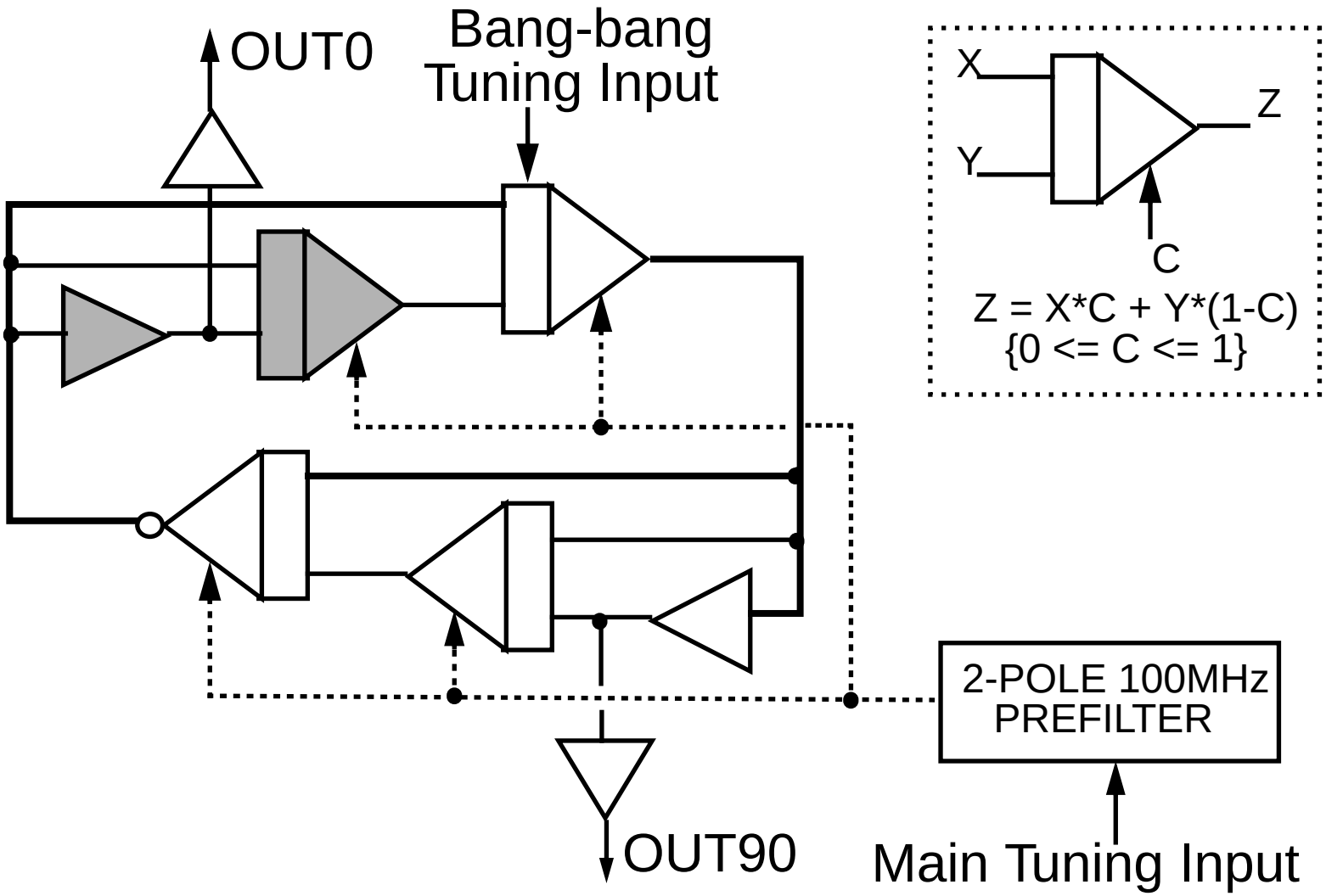
Typical Synchronous Optical Network (SONET) RX “Front-end”



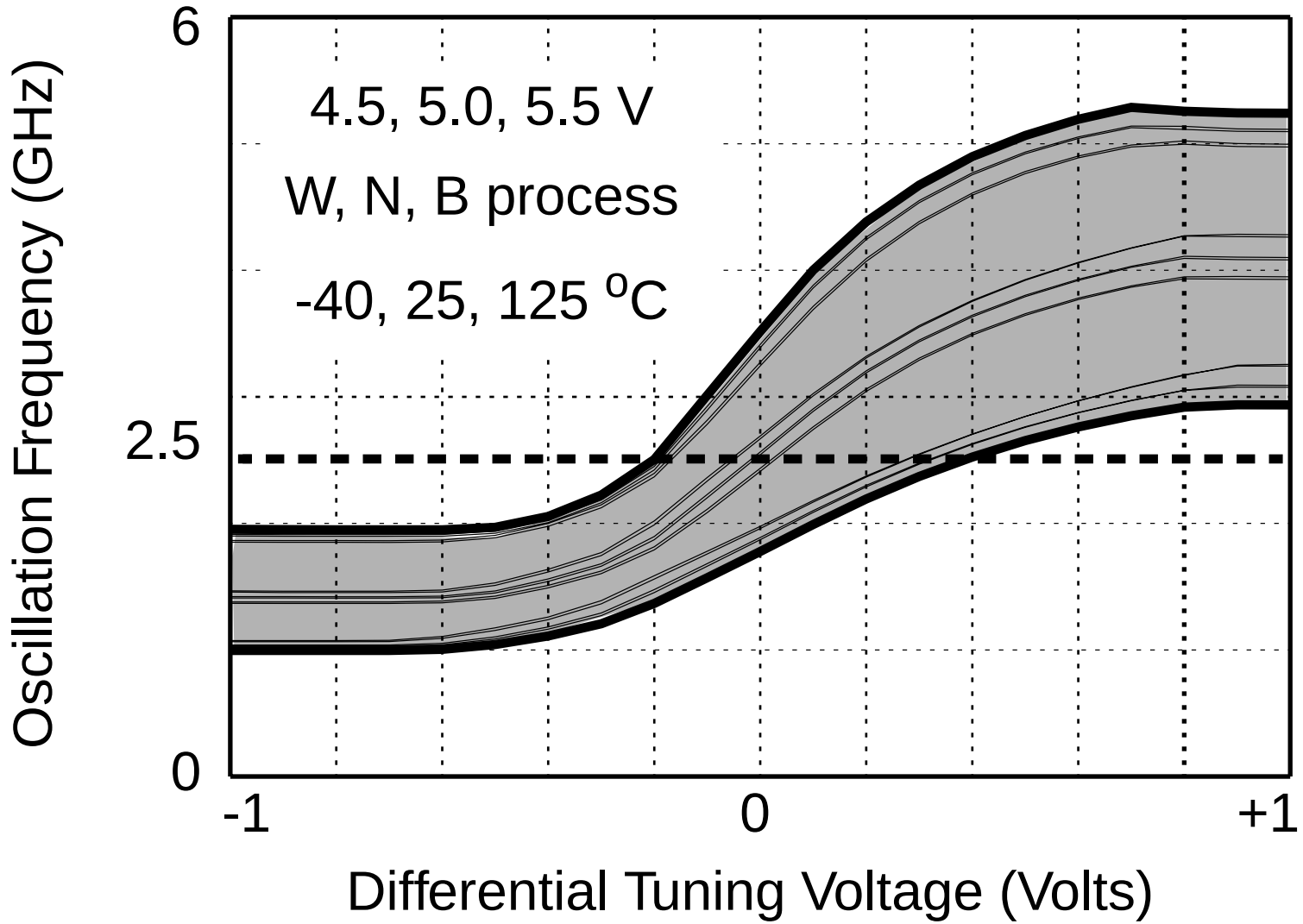
Design Goals

- Monolithic Implementation
- Adjustment-Free Manufacture and Operation
- Reliable Loss-of-Signal (LOS) Threshold
- Meet all SONET Jitter and Reliability Specifications

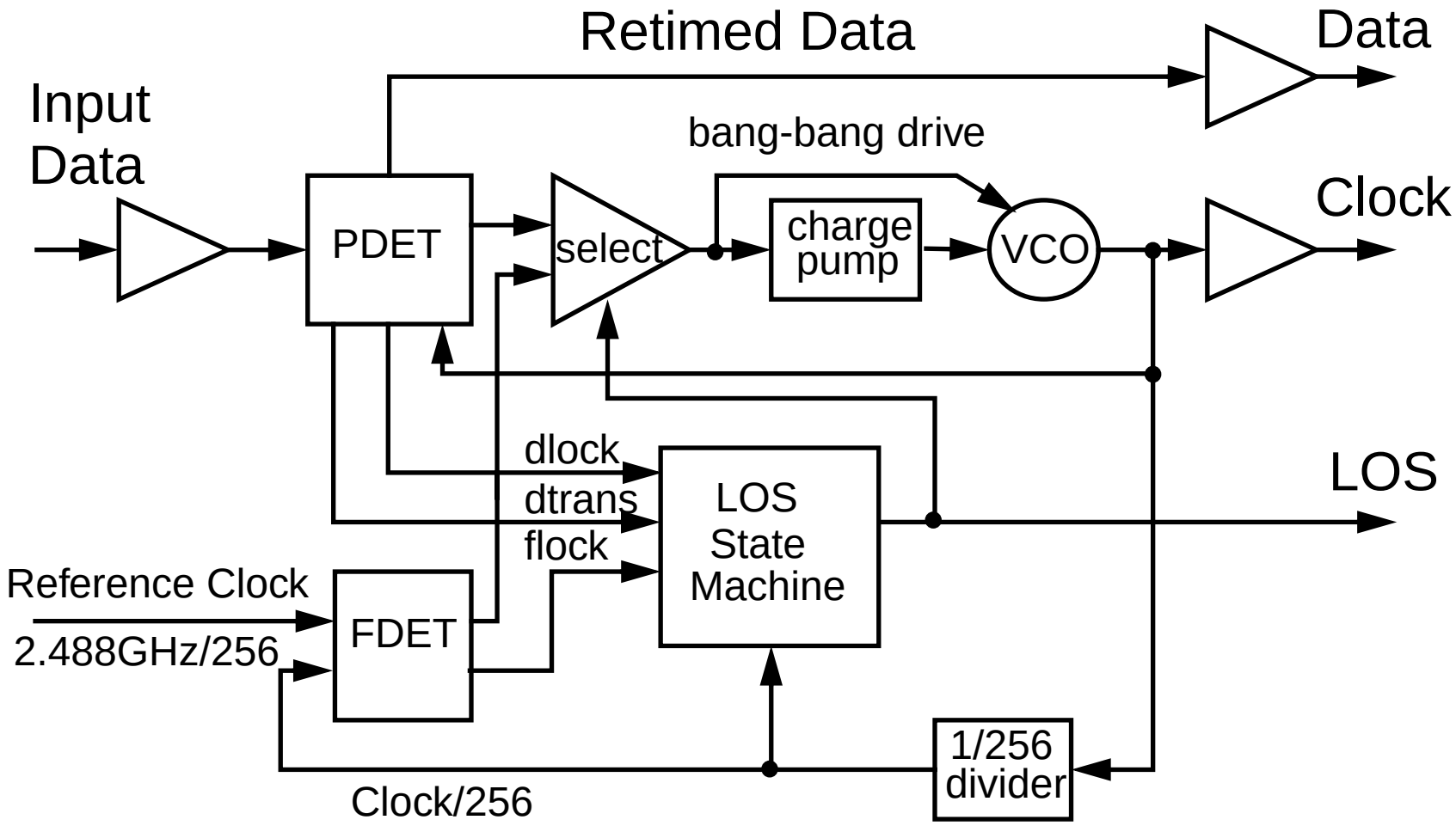
Ring Oscillator VCO



Simulated VCO Tuning Curves



Chip Block Diagram

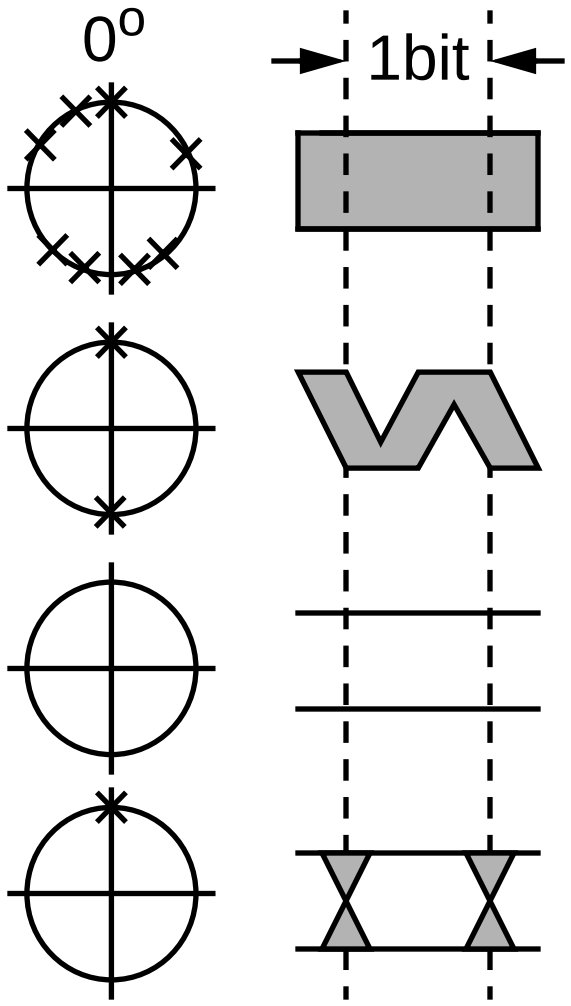


Loss-of-Signal (LOS) Requirements

Must operate *reliably* on a defined Bit-Error-Rate (BER) threshold and not be “fooled” by:

- Random transitions from noisy transimpedance amp (x-amp)
- Coherent, double-speed transitions due to feedback of VCO energy into the x-amp
- Stuck at 1, or 0 level due to input offset or hysteresis in limiting amplifier chain

Normal Data Eye:

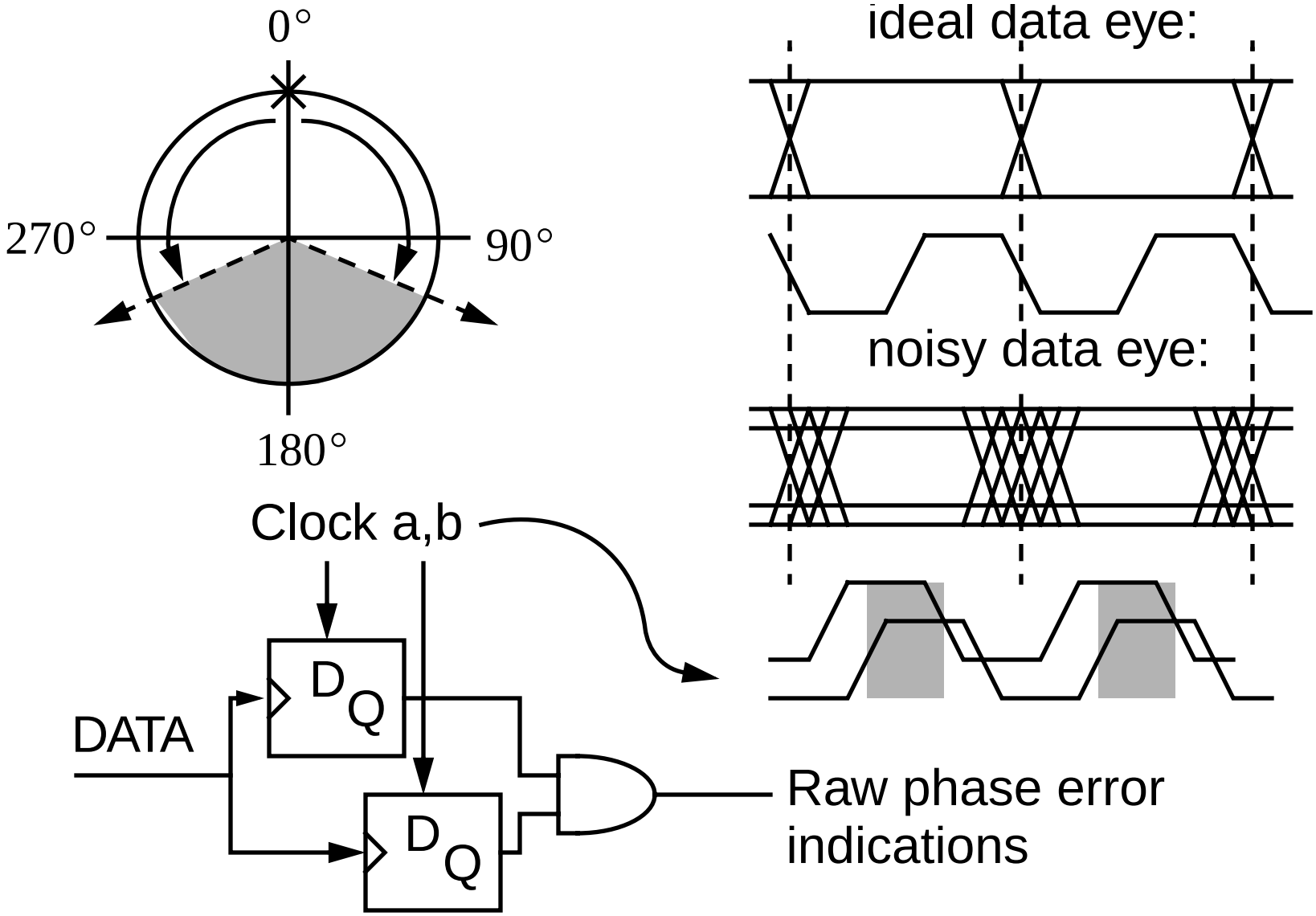


Reliable LOS detection

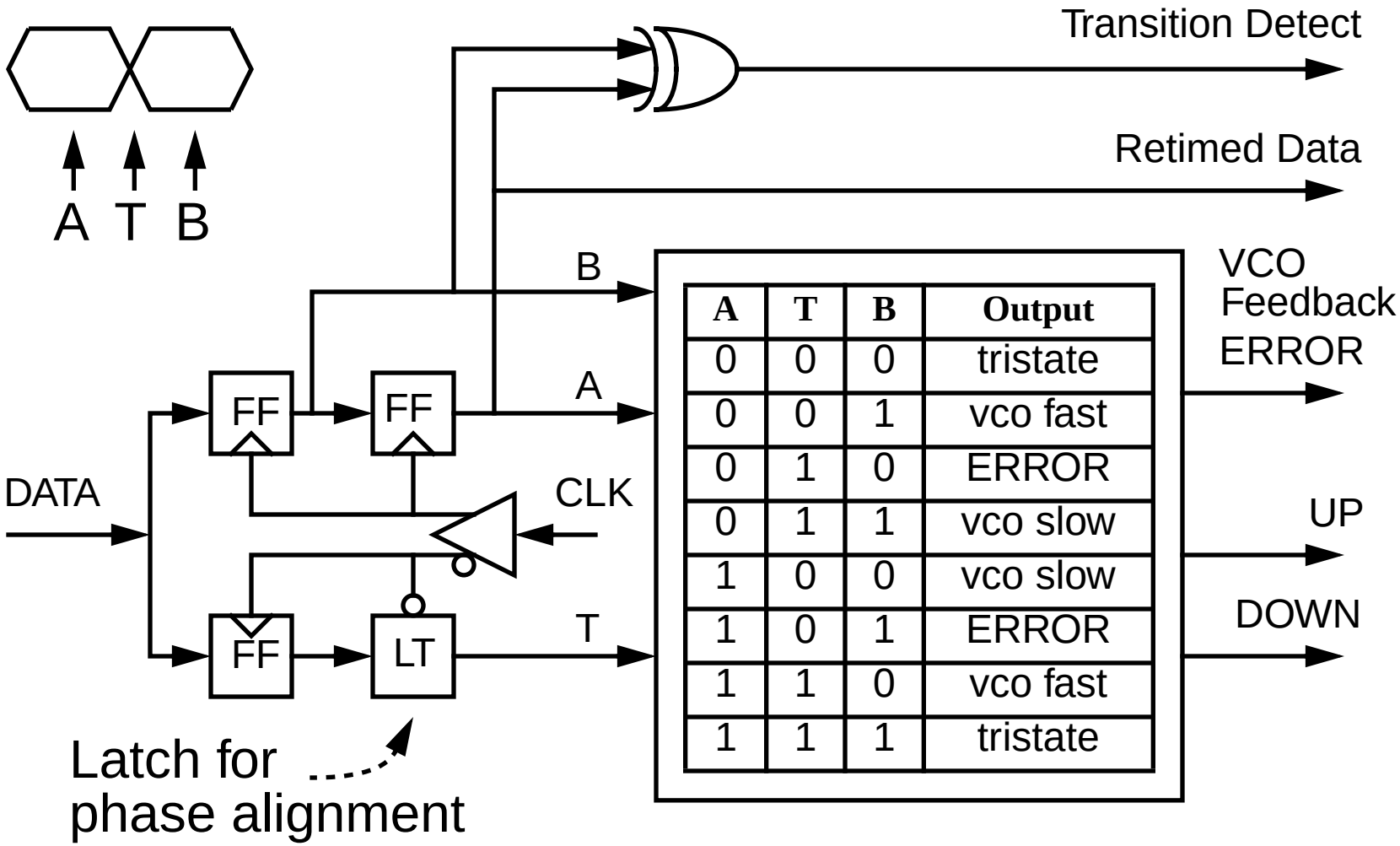
Can’t know actual Bit-Error-Rate (BER), so:

- Assume that Phase Jitter is Proportional to BER
- *Reliable* means that:
  - Mean Time to Restarting (MTTR) is less than one *second* at target BER threshold
  - MTTR is greater than one *year* when BER improves by 2 decades over threshold
  - Statistical Processing of Raw Errors will be required for reliable “snap-action” operation

Data-Lock Detection

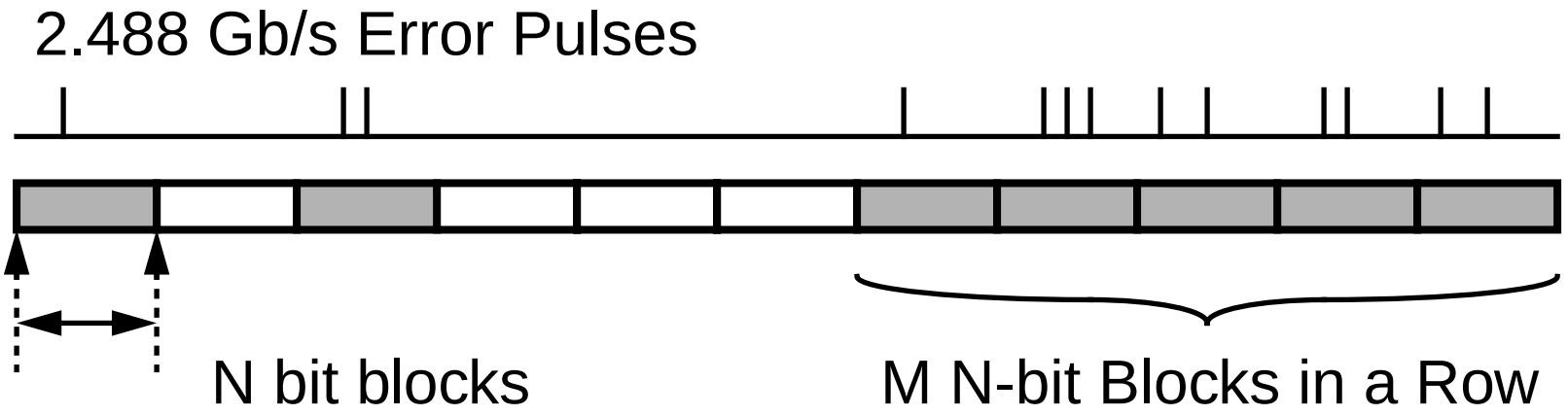


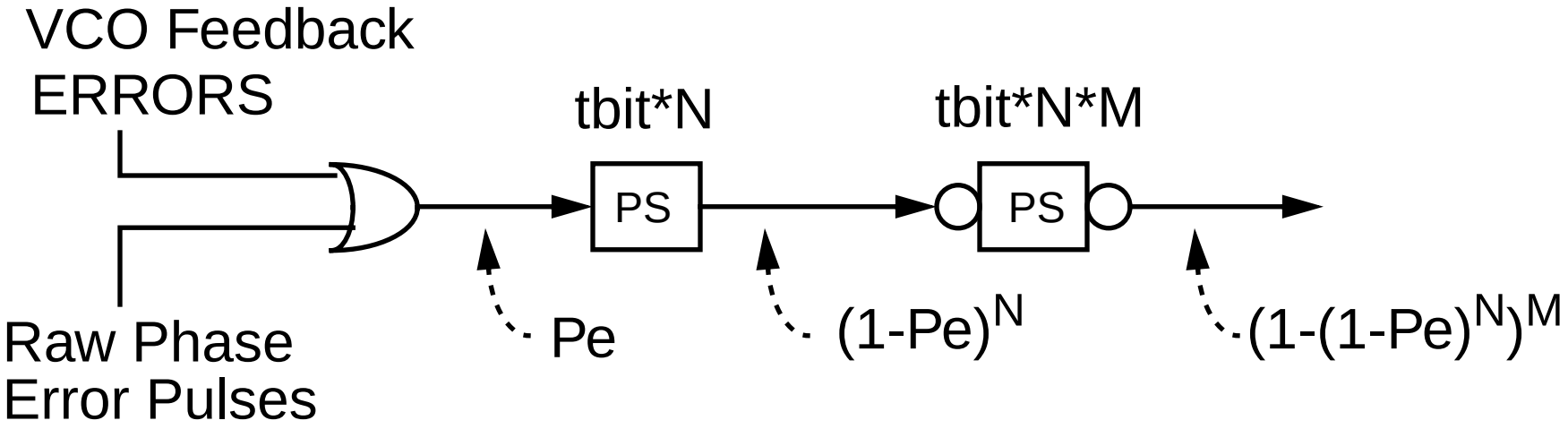
Phase, Transition and VCO-feedback detection



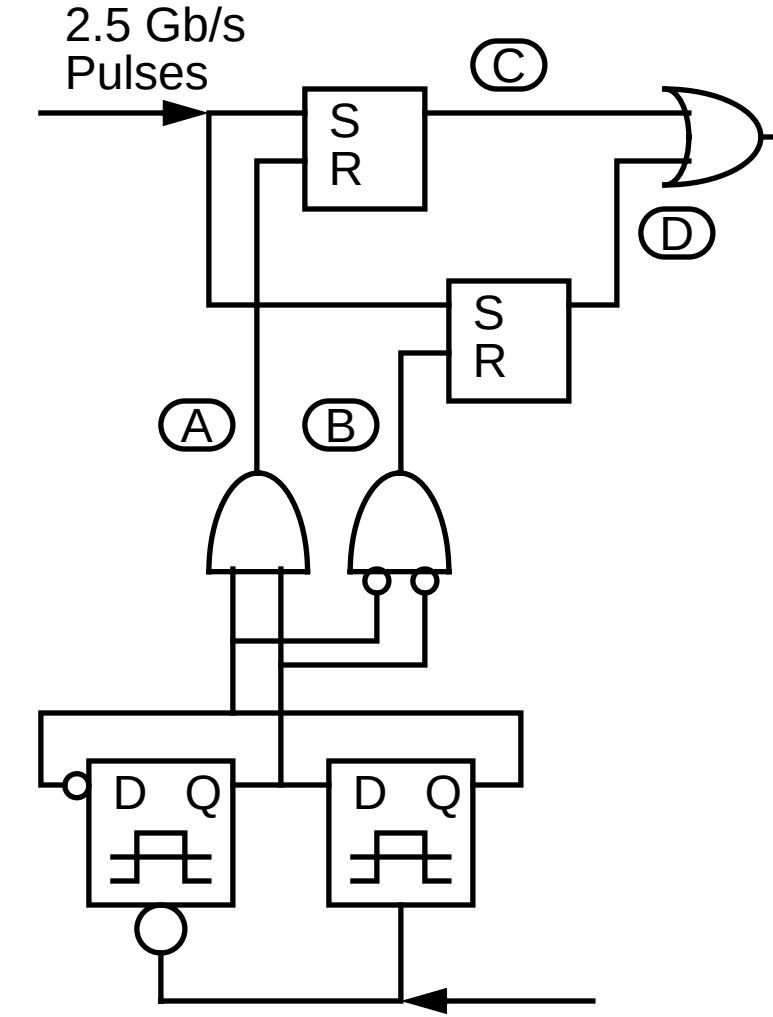
A	T	B	Output
0	0	0	tristate
0	0	1	vco fast
0	1	0	ERROR
0	1	1	vco slow
1	0	0	vco slow
1	0	1	ERROR
1	1	0	vco fast
1	1	1	tristate

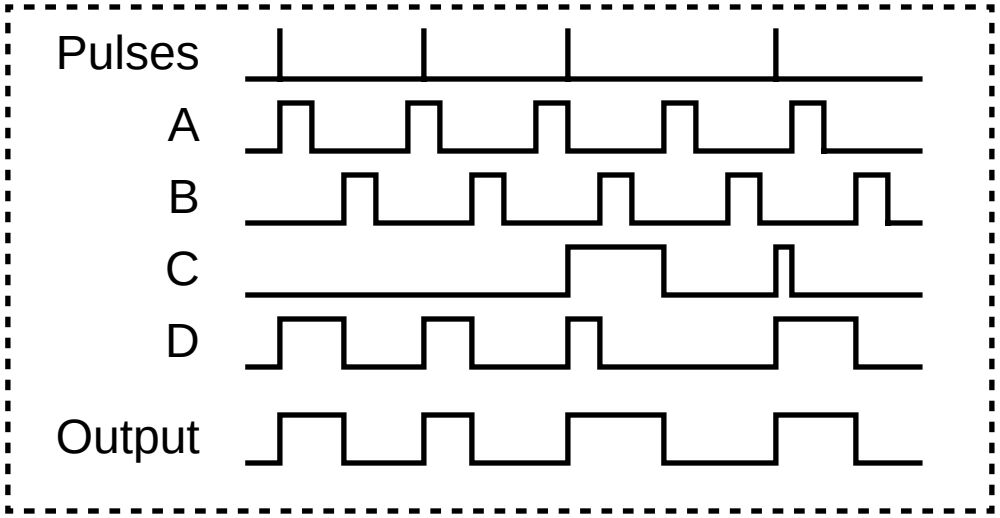
Error Qualification Strategy





Pulse Stretcher Circuit

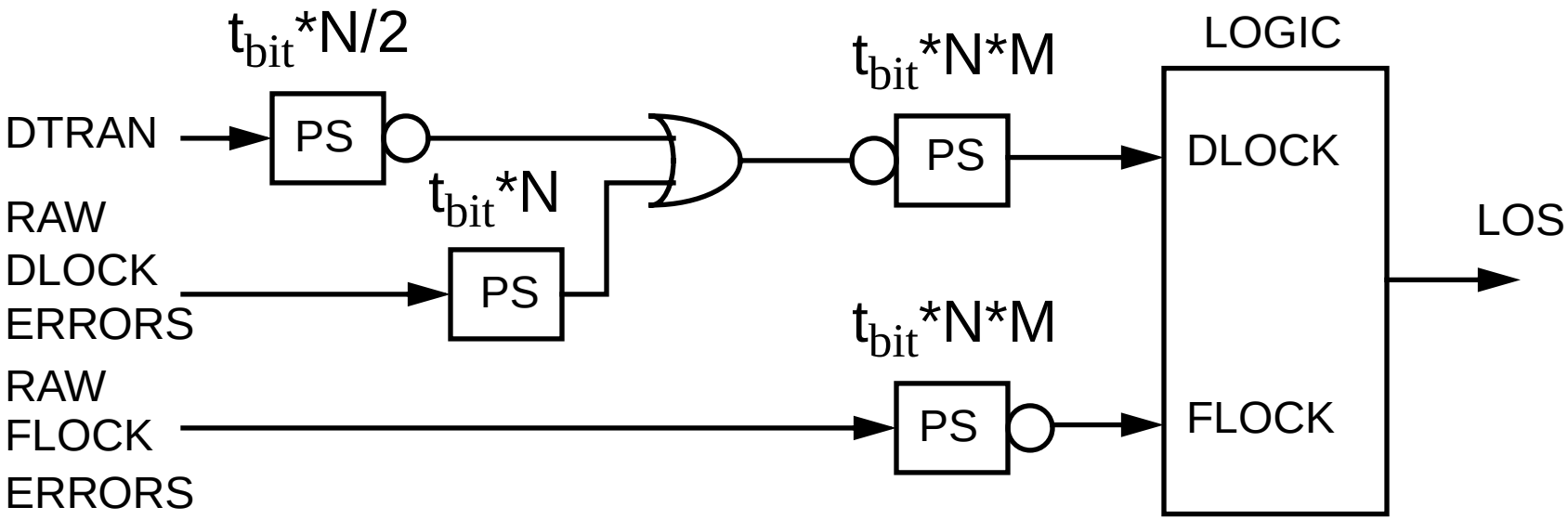


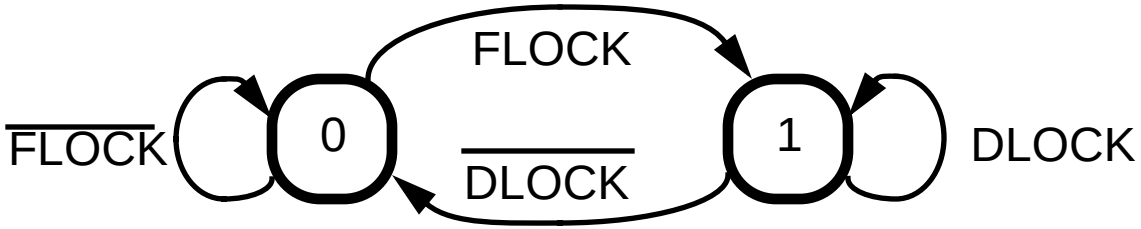


Stretches 400ps input pulses to ~10uS output pulses for low-power logic processing.

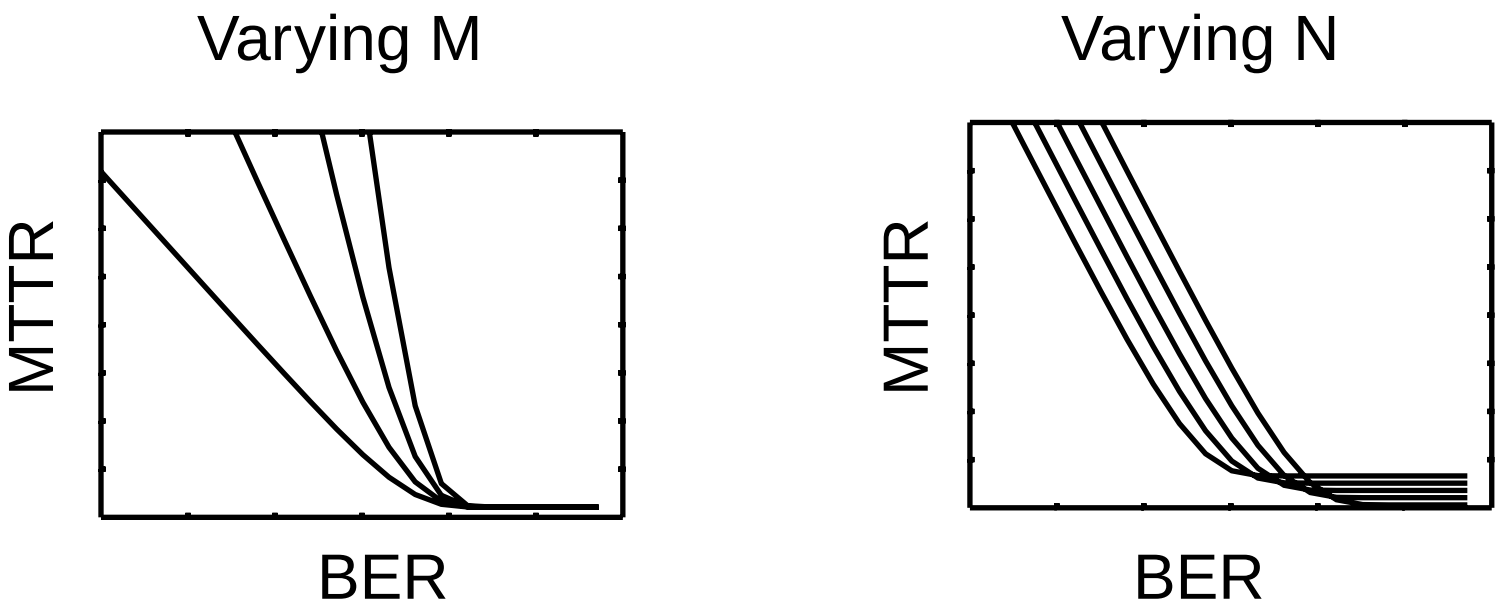
Acts like a monostable multivibrator with 2/fc < Tstretch < 6/fc

LOS Circuit


t_{bit}*N/2
t_{bit}*N*M
LOGIC
DTRAN
PS
t_{bit}*N
PS
DLOCK
RAW
DLOCK
ERRORS
PS
LOS
t_{bit}*N*M
RAW
FLOCK
ERRORS
PS
FLOCK


FLOCK
FLOCK
0
1
DLOCK
DLOCK

LOS performance vs M,N

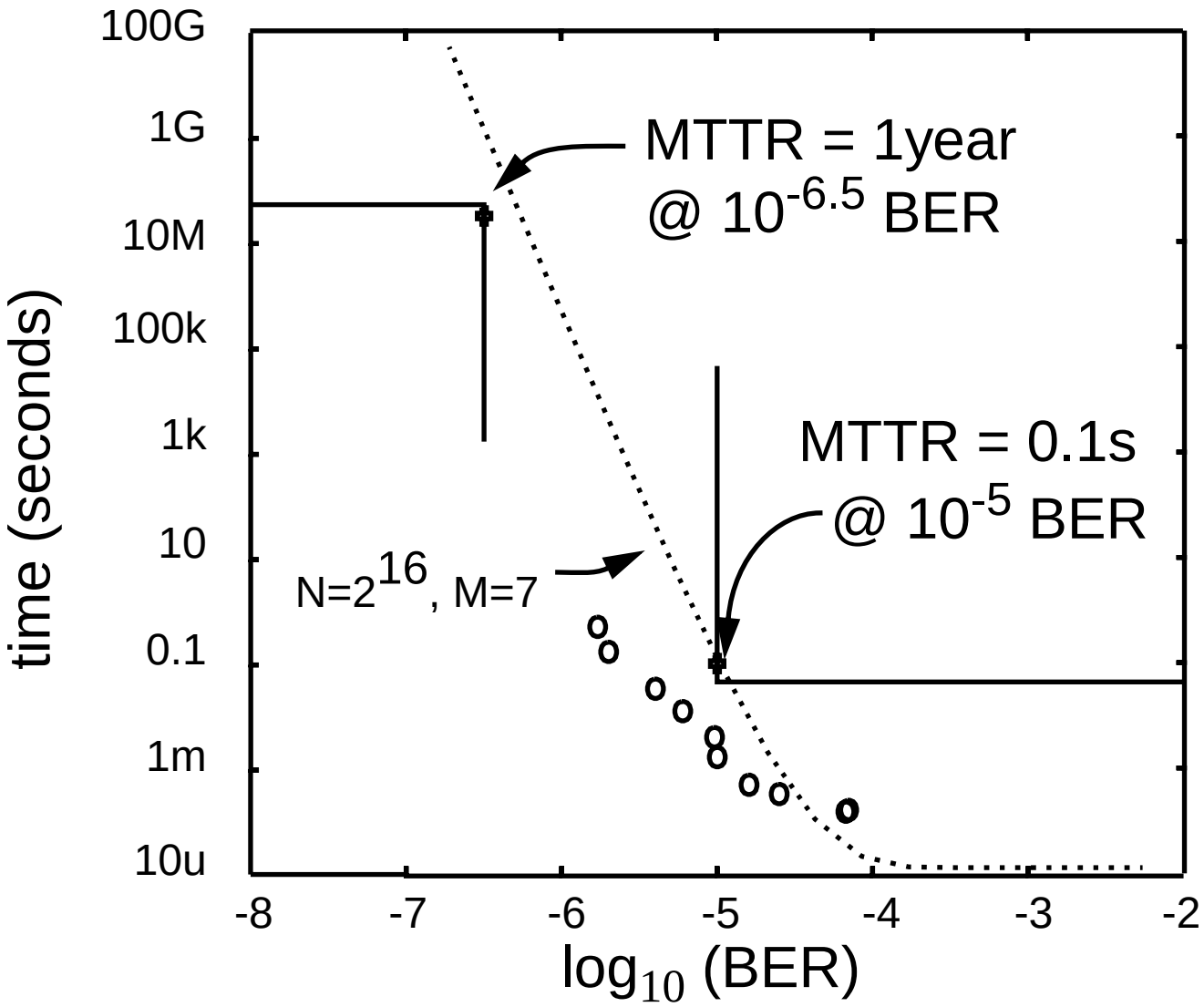


- Architecture allows independent control of both slope and threshold

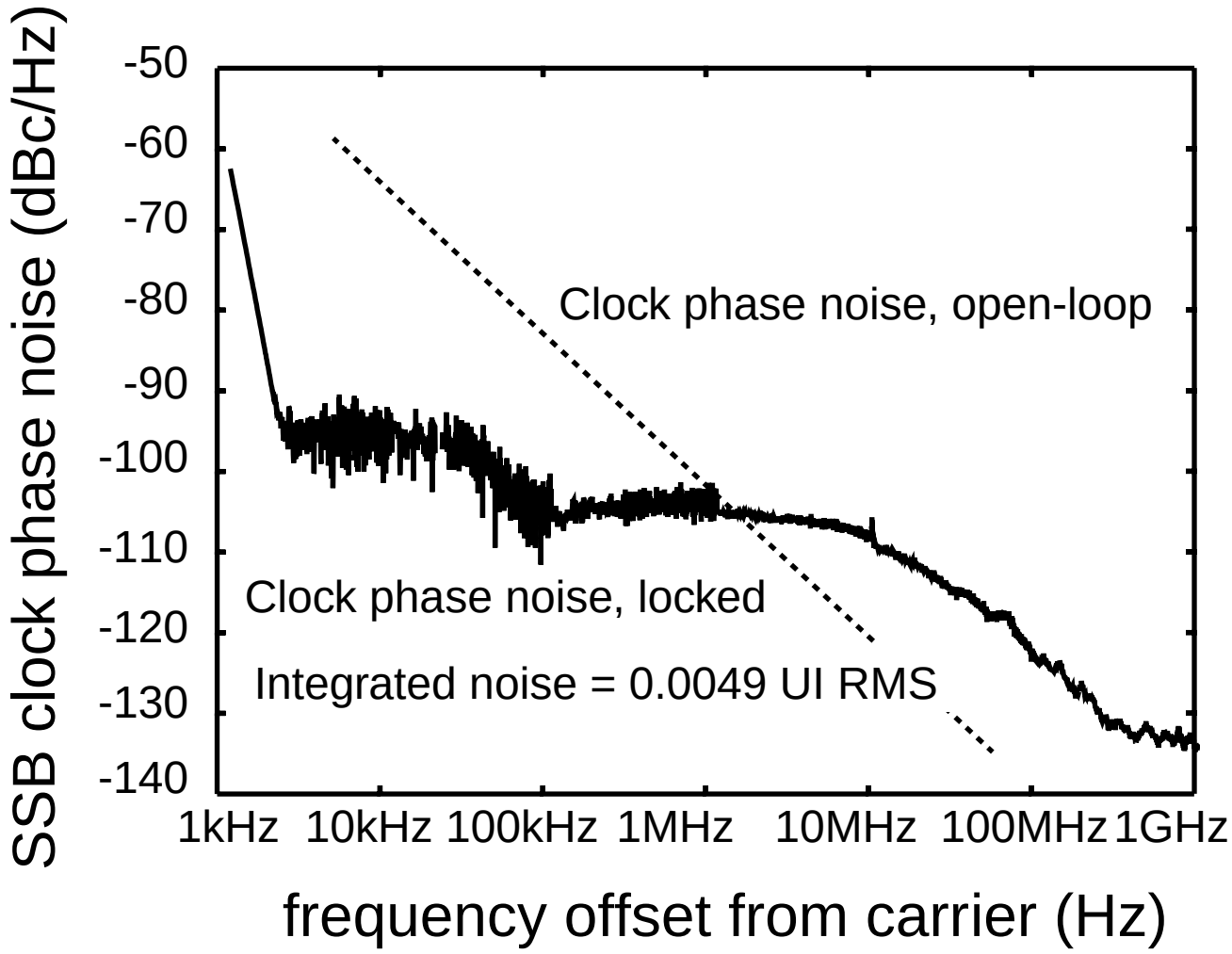
Measured Results

- MTTR vs BER
- Clock Phase Noise
- Clock and Data Waveforms
- Packaged Part
- Summary of Key Specifications

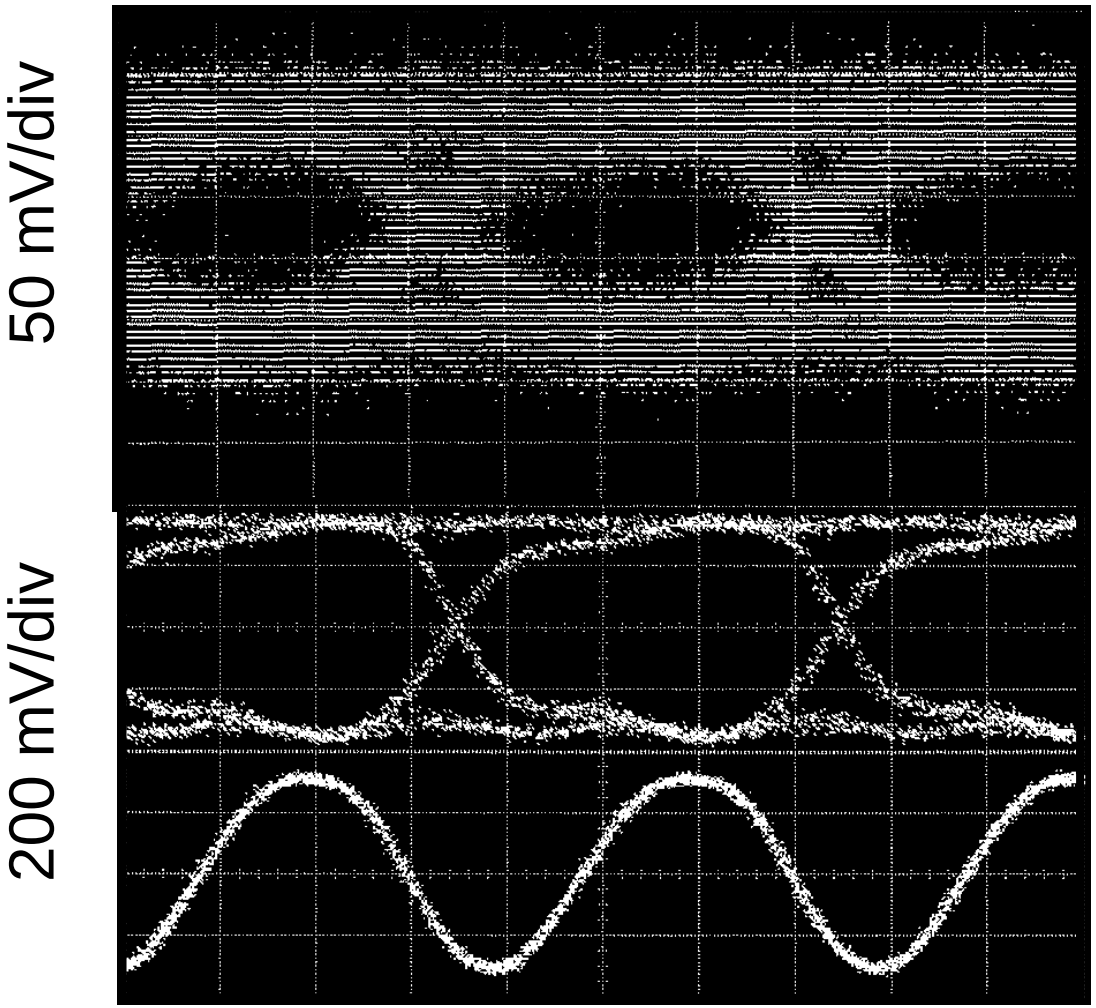
Measured MTTR vs BER



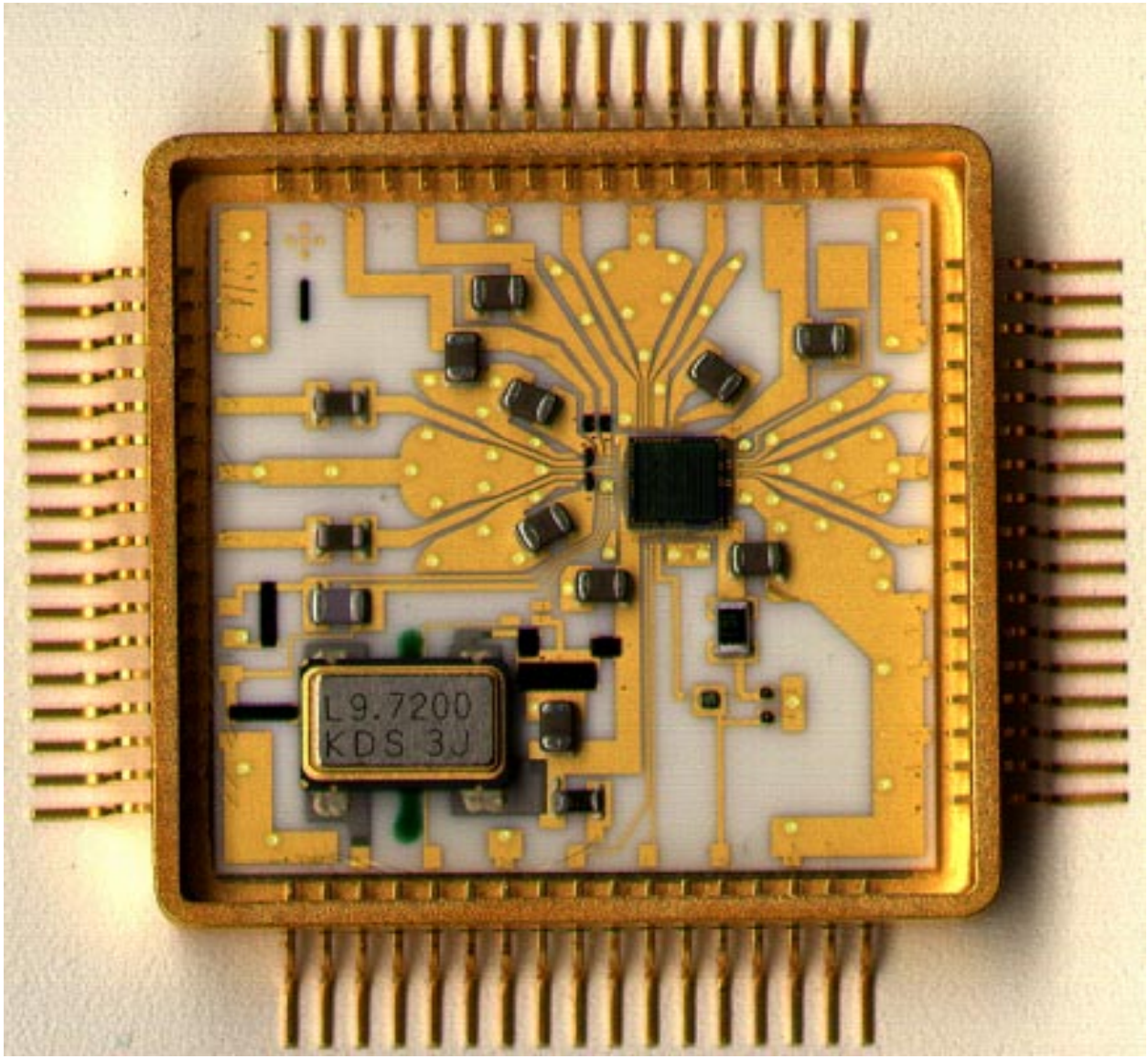
Measured Clock Phase Noise



Measured Clock/Data Waveforms



Packaged Part



Summary

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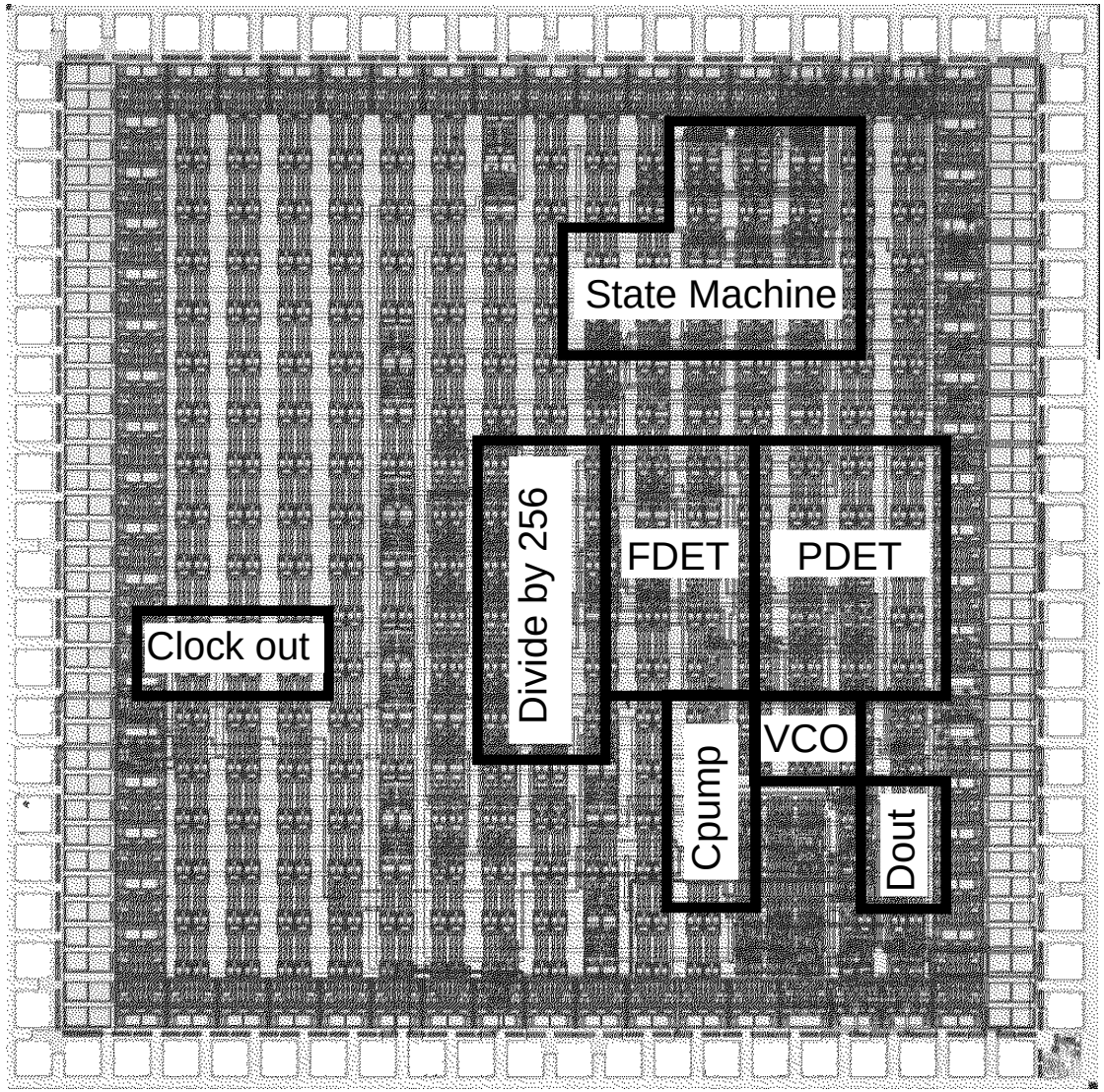
Parameter	Value	Units
Guaranteed Frequency Range	2-3	Gb/s
Supply voltage	4.5-5.5	V
Supply current (nominal)	340	mA
Power dissipation	1.77	W
Case temperature range	0-60	°C
Die size (gate array)	3.45x3.45	mm^2
Number of active devices	3606	
IC Process	25 GHz f_T Si-Bipolar	
Jitter Generation	0.0049	UI (rms)
Jitter Tolerance	meets SONET Spec	

Die Photo


State Machine
Divide by 256
FDET
PDET
Clock out
VCO
Cpump
Dout