A Monolithic High-Speed Voltage Controlled Ring Oscillator

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Abstract

A new topology for a monolithic VCO is presented. A 3 element ring oscillator is merged with a 5 element ring oscillator by using a linear combining circuit. By adjusting the control voltage, the oscillation frequency can be varied from $1/(2\times3\times T_{gate\_delay})$ to $1/(2\times5\times T_{gate\_delay})$. The circuit concept requires no off-chip parts, and can be extended to greater than 1 octave tuning range.

Experimental results are presented for the oscillator implemented in the HP RFIC GaAs process. Measured frequency range was 1.4 GHz to 2.4 GHz. Power dissipation was 1.3 Watt, with die size of .5x.5 mm. Simulation results are also given for an HP1X bipolar implementation.

These chips are intended to be used as clock sources for a digital data link timing recovery circuit.

1. Introduction

Voltage controlled oscillators are widely used in communication systems. For cost reasons, it is always desirable to minimize both chip count and the number of external parts needed to build a given system. The following oscillator design fulfills these needs by being integrable on the same chip with other functions and requiring no external frequency determining elements. The oscillator described is rapidly tunable and thus capable of wideband FM or PM. Other rapidly tunable VCO designs, such as Schmidt trigger oscillators, operate in a saturated switching mode and are consequently limited in speed [1]. Ring oscillators, in contrast, may be operated in a non-saturating mode up to very high frequencies.

2. Background

A conventional ring oscillator is shown in figure 1. The ring consists of an odd number of inverting stages. This constraint ensures that the oscillator will self-start. If a rising logic edge propagates around the ring it will, after one round trip, become a falling edge. After two such round trips it will be a rising edge again. If the delay of a gate is T_d, then the frequency of oscillation will be $1/(2T_dN)$; where N is the number of stages in the loop.

Ring oscillators used for process characterization typically consist of a large number of inverters. This is done to ensure a saturated logic swing to realistically test the digital performance of the process. The oscillators described in this paper differ in that they consist of a small number of inverters and run in a quasi-linear mode with near sinusoidal waveforms.

3. Circuit Operation

A description of the new circuit is based on figure 2. The functional block labeled M is unconventional. Output V_z is a linear combination of inputs V_x and V_y. The combination coefficients are controlled by an input C; where $0 \le C \le 1$. If $V_x(t), V_y(t)$ are the voltages at ports V_x and V_y, then the output voltage $V_z(t)$ is given by

$$V_z(t) = CV_x(t) + (1 - C)V_y(t) \tag{1}$$

The output of the M stage is a weighted sum of two sinusoids that are of the same frequency but different phases. The sum is also a sinusoid with a phase (and delay) that can be found from the phasor diagram shown in figure 3. Consider the two special cases where $C = 0$ and $C = 1$. In the first case $V_z(t) = V_y(t)$. Figure 2 then reduces to a three element ring oscillator consisting of inverters 1,2 and 5. This gives an oscillation frequency of $1/(2 \times 3 \times T_d)$ Hz. In the second case, $V_z(t) = V_x(t)$, giving a five element ring, and an oscillation frequency of $1/(2 \times 5 \times T_d)$ Hz. The resulting tuning range ratio is then 5/3.

In order for the circuit to work correctly when C is an intermediate value, two conditions must be met. First, the waveforms must be approximately sinusoidal. This is normally the case when there are a small number of stages since the resulting oscillation is near the maximum speed of the inverters. Second, the waveforms at V_x and V_y must have less than 180° of phase shift between them (preferably close to 90°). We will now assume the second condition and prove it later in equation (6).

The circuit will oscillate at a frequency where there is exactly 360° phase shift around the loop. There is already 180° due to the inversion in the loop, so the oscillation frequency is where the propagation delay contributes an extra 180°. The phase shift due to inverters 1,2 and 5 is fixed, while the phase shift due to the combination of inverters 3, 4 and the M stage is adjustable. If we let ϕ be the phase difference between $V_x(t)$ and $V_y(t)$, then the waveform at the output of the M cell is

$$V_z(t) = C\sin(\omega t - \phi) + (1 - C)\sin(\omega t). \tag{2}$$

The phase of this waveform is

$$\Theta = \tan^{-1}\left[\frac{C\sin\phi}{(C-1) + C\cos\phi}\right] \tag{3}$$

Equation 3 is somewhat intractable, but can be approximated to first order with acceptable error for $\phi \le 120°$ by

$$\Theta \approx C\phi. \tag{4}$$

The total loop phase shift is then $C\phi + 3 \times 2\pi f_{osc} T_d$. Substituting in for $\phi = 2 \times 2\pi f_{osc} T_d$ and setting the loop phase shift equal to π gives the oscillation frequency:

$$f_{osc} \approx \frac{1}{(6 + 4C)T_d}. \tag{5}$$

We can now verify our initial requirement that $V_x(t)$ and $V_y(t)$ have less than 180° phase shift between them. The phase shift between $V_x(t)$ and $V_y(t)$ caused by the two inverters is,

$$\phi = \frac{360°}{3 + 2C} \le 120° \tag{6}$$

4. GaAs RFIC Results

Figure 4 shows the oscillator implemented in GaAs. The tune line labeled "C" is differential. The output is tapped off of inverter 4 to minimize loading on the high speed ring consisting of inverters 1, 2 and 5. Figure 5 shows the measured frequency versus tune voltage. Results are summarized in Table 1. As has been seen in other low Q GaAs oscillator designs, the circuit has relatively poor spectral purity [2]. The output spectrum shows $1/f$ components about the carrier. This is probably due to the high $1/f$ noise corner of the GaAs FET's used. For the intended use in a clock timing recovery circuit, the oscillator will be phase locked to an incoming signal. The short term stability of the oscillator is then sufficient to properly sample data between adjustment periods.

5. Si Bipolar HP1X Simulations

An oscillator of the type described was also designed in the HP1X bipolar process. The inverter stages were implemented with fully differential ECL. Figure 6 shows the circuit for the *M* stage along with a representative inverter. Simulation results are also shown in Table 1. It is expected that the bipolar version will have better phase noise performance than the GaAs version, due to the better $1/f$ noise of the Si devices.

Table 1. Summary of Results		
Parameter	RFIC GaAs (measured)	HP1X (simulated)
circuit area	.5x.5mm	.05x1.7mm
power	1.3 watt	0.1 watt
yield	>95%	-
tuning range	1.4GHz - 2.4GHz	634MHz - 1.08GHz
phase noise	-40dBc@500KHz	-
output amplitude	12dBm	0dBm

6. Extensions to the Concept

The basic topology of the oscillator may be extended to have higher tuning range as shown in figure 7. This modification allows tuning ranges of 3/7, 3/9, etc. The use of multiple *M* stages is required to keep the phase difference at the input of each *M* stage less than 180°. The practical limit with this topology is reached when the resulting waveform is no longer approximating a sinusoid. This limit will be a function of the technology used.

7. Summary

A technique for making monolithic high-speed VCO's on both GaAs and silicon IC's has been described. The circuit described has the following advantages:

1) Can be operated at very high speeds
2) Fully integrable along with digital circuitry
3) Large tuning range and rapid frequency adjustment
4) No external frequency determining elements required

8. References

[1] Alan B. Grebene, *Analog integrated Circuit Design,* Van Nostrand Reinhold Company, New York, 1972, pp. 331-315.

[2] R. L. Van Tuyl, "A Monolithic GaAs IC for Heterodyne Generation of RF Signals," *IEEE. Transactions on Elecron Devices,* vol ED-28, no. 2, Feb. 1981.