A 46 I/0 Package for Prototyping Multi-GHz Circuits

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ABSTRACT

A high frequency prototyping package with 46 SMA I/O's is described. The package size is 8.5" x 9" and has a bandwidth greater than 10 GHz. The signals are coupled from the teflon microstrip to the test hybrid using the Tektronix "HYPCON" connector. The HYPCON connector consists of a rubber gasket with small gold contacts bonded to it which is held in a plastic frame. The hybrid assembly may be easily replaced in a few minutes by removing and replacing the HYPCON connector. The delays in each of the 46 lines were equalized to the center of the hybrid to help with testing. Provision was made to allow die attaching the hybrid assembly to the baseplate to aid in heat dissipation.

Introduction

This report describes a high frequency, large I/O count, prototyping package developed in the HPL Instrument Technology Department. This package was developed for use in testing the high speed integrated circuits designed in this department. Although packaging is not our normal activity, we found it necessary in order to fulfill our needs. Existing microwave packages did not provide enough signal I/O's, while PGA's, flatpacks, etc., did not provide good high frequency performance. We hope that others faced with similar needs will be able to use or alter what we have done to suit their requirements.

The report consists of five sections. The first section describes the goals set for the package, and is followed by a section describing the package itself. The third describes a generic hybrid developed for use with the package. The fourth and longest section describes in detail the measured performance of the package. Included is a SPICE model that accurately models package performance. The conclusion summarizes our results and lists areas for further work.

1. Goals for the Package

Two features of the package were considered to be necessary: high performance, and high I/O count. Several digital IC's designed in our group require at least 20 signal I/O's, and 10 DC feeds. Rise times on the order of 50 ps, and bandwidths of roughly 9 GHz are needed to fully test these circuits.

Unit cost, long "lifetime" (thermal cycling, humidity sensitivity, thousands of reconnects), size and weight were not considered strong factors because this is a lab prototyping package only.

Additional goals were prioritized as follows:

• Reliability

Ideally the package should never require tweaking or adjustment, and should never fail to make connection even when it is moved or shocked.

• Flexibility

Many different types of analog and digital IC's are being developed in this department. In addition, we are working on systems requiring several IC's to be closely interconnected, as well as circuits containing discrete microwave devices. If one package could serve all these needs, it would save a lot of time, effort, and expense.

• Heat Dissipation

One chip already being tested dissipates four Watts on a 2 x 2.6 mm die. Even higher power densities are considered likely in the future. The package should handle these powers with minimum temperature rise at the chip.

• Ease of Use

It should be quick and easy to replace the circuit in the package. This is necessary for comparing circuits, quickly replacing damaged circuits, or sharing the package between projects. It should also be convenient to connect the instruments and power supplies being used to test the circuit.

• Equalized Delays

For ease in testing and measuring circuits, it is convenient if all signal paths have the same time delay from the circuit to the connectors on the package. This is particularly important if differential signals are being used, or if skew between channels is one of the parameters to be measured. Note that at 5 GHz a 1.5 cm path length difference causes a 180 degree phase shift.

2. Package Description

Figure 1 shows a conceptual diagram of the the package. The package is based on a connector made by Tektronix called the "HYPCON" [1,2]. The HYPCON connector is priced at $14 to $20 in 100 quantity. It is composed of a rectangular rubber gasket, which is pressed down by a plastic frame. Figure 2 shows a cross section of the HYPCON in use. On the rubber gasket are metal tabs the same width as the traces on the PC board. When correctly aligned and tightened down, these metal tabs provide a conduction path from a 50Ω trace on the PC board to a 50Ω trace on the hybrid. Note that the surface of the hybrid and the surface of the PC board must be at the same level in order for this to work. Both the hybrid and PC board are 10 mils thick, so the surface below them merely needs to be flat. SMA connectors are arranged in an oval, providing equal time delays to the center of the 1" x 2" hybrid for all 46 traces. All 46 traces are 50Ω lines, and can be used as signal lines or DC feeds, depending on the hybrid design. SMA connectors make contact to the PC board traces via their center pins, which come up through the PC board from the bottom. The chip being tested is connected to the hybrid by wire bonds. The base plate is 8.5" x 9.0" x 0.25". The physical parameters of the various microstrip lines are given in Table 1.

Table 1. Microstrip Parameter Values

	Teflon microstrip (PC)	Sapphire microstrip (Hybrid)
Substrate Thickness	10 mil	10 mil
Trace Thickness	.0029" (Cu,Ni,Au)	.00012" (Au)
Trace Width	27.5 mil	10 mil
Dielectric Constant	2.45	10
Delay (% of c)	.7	.3

Hybrids can be quickly removed and installed by unscrewing the HYPCON frame and lifting them in or out. The HYPCON frames have small corner pegs that insure correct alignment of the hybrid, PC board, and the HYPCON's metal tabs.

For most of our low power applications, the hybrid may just be placed into the package with no heat sink grease or other precautions. For better higher power circuits, the hybrid may be die attached to the removable pedestal. If a 2 x 2 mm die that dissipates 10 Watts is die attached to the hybrid, and the hybrid die attached to the pedestal, the temperature rise to the back of the chip is estimated to be 21° centigrade. Table 2 shows a listing of the temperature rise across various layers that might be encountered in a package. For each example, a heat flux of 2. 5 Watts/mm^2 is assumed.

Layers joined with heat conducting epoxy or thermal grease are clearly unacceptable. The temperature rise across the alumina substrate is tolerable. Thus if the chip is die attached to the hybrid, and the hybrid die attached to the metal pedestal, the temperature rise is acceptable for high power dissipation chips. Even better heat conduction could be obtained from beryllia substrates.

Because it may be necessary to use expensive materials for the pedestal (such as covar or titanium-copper) to match the thermal expansion properties of the substrate, an effort was made to make this part small, simple, and therefore inexpensive. This is especially important considering that a pedestal may be die attached to only once before the gold plating is leached off by the solder.

Table 2. Thermal drops for various materials			
Material	Thickness	Thermal Conductivity	ΔT
Alumina	.025 cm	.36 W/cm°C	$17°C$
Beryllia	.051 cm	2.0 W/cm°C	$6.4°C$
Die Attach	.0025 cm	.34 W/cm°C	$1.8°C$
Epoxy (insulating)	.0025 cm	.0046 W/cm°C	$136°C$
Epoxy (conducting)	.0025 cm	.018 W/cm°C	$35°C$
GaAs	.025 cm	.59 W/cm°C	$11°C$
Silicon	.051 cm	.98 W/cm°C	$13°C$
Thermal Grease	.0025 cm	.0023 W/cm°C	$272°C$

Since a hybrid cannot be die attached in an exact position on the pedestal, the pedestal was designed with some adjustment "slop" for aligning the hybrid with the hole in the PC board. The pedestal is made so that its surface is exactly level with the baseplate. Note that the gap between the pedestal and baseplate occurs under the PC board, away from the critical HYPCON connection.

3. Generic Hybrid

While it is possible to design a custom hybrid for each circuit, we found it useful to have a generic hybrid substrate that could be used to test a wide variety of circuits. A plot of a hybrid design with the following features is shown in Figure 2.

- 38 total lines
- 30 possible terminated 50 Ω lines
- 16 possible DC lines with bypass capacitors
- 3 mm x 3 mm die attach area

Some of the lines can be used as either terminated AC lines or bypassed DC lines. The 50 Ω terminations are optionally included as a bonding option. The resistors are connected between ground and a small pad which can be bonded to the 50 Ω micro-strip. The terminations are located between the die attach area and the signal lines. Conductive vias are used to make ground connections. DC feed bypassing is accomplished by epoxying chip capacitors between ground and the signal trace. This hybrid has been fabricated at MWTD in the thin-film TF-II process on a sapphire substrate.

The cost of this hybrid was rather high ($700/each). This is due to the large size of the substrate, with consequent low yield, coupled with the low volume fab line at MWTD. We are exploring other materials and vendors to find a more cost effective solution. A thick-film ceramic hybrid with slightly reduced performance has the potential of costing less than $20 per substrate.

4. Measurement Results

The key figure of merit is the package-induced rise-time degradation of signals as they propagate either on or off chip. Due to the difficulty of observing very high speed signals on the hybrid substrate, it is necessary to arrive at this measurement in an indirect fashion. The approach that was taken was to develop an electrical model from external loop-thru measurements which could then be "cut in half" to simulate the performance on the hybrid.

Time Domain Reflectometry (TDR) measurements were made on the package along with Frequency and Pulse response of a thru path. For these measurements, the signal is coupled from an SMA connector onto the PC board microstrip, across the HYPCON interface, through the hybrid microstrip and then back off through a similar path. The response of the thru TDR measurement is shown in Figure 4. This plot, in conjunction with a rise time measurement of the TDR probe step, allows the equivalent lumped values for major discontinuities to be calculated. For a probe step rise time (τ) and a perturbation (ρ), the following equations were derived:

$$\rho_{peak} = \begin{cases} \dfrac{L}{2Z_0\tau}\left(1 - e^{\frac{-2Z_0\tau}{L}}\right) & ;\ \text{for positive discontinuities} \\ \dfrac{Z_0C}{2\tau}\left(1 - e^{\frac{-2\tau}{Z_0C}}\right) & ;\ \text{for negative discontinuities.} \end{cases}$$

For discontinuities below 200 $m\rho$, the exponential term in the above expressions may be neglected with less than a 1% error. We used these simplified formulas to help develop an equivalent SPICE model for each discontinuity.

The discontinuities at the HYPCON were caused by the fact that the tab was wider than a 50Ω line. The HYPCON overlap on the sapphire substrate was 50 mils x 26 mils. A program was written to calculate microstrip properties from various physical parameters and dimensions based on reference [3]. The program was used to determined that the HYPCON overlap was equivalent to a transmission line segment with a delay $\delta = 111$, and an impedance $Z_1 = 26.4\Omega$. Using the relationship that $C_1 = \delta / Z_1$ and $L_1 = Z_1 \delta$, we can compute the equivalent lumped discontinuity of the line to be

$$L_{lumped} = \frac{(Z_1{}^2 - Z_0{}^2)\delta}{Z_1} \quad ;\ \text{for positive discontinuities}$$

$$C_{lumped} = \frac{(Z_0{}^2 - Z_1{}^2)\delta}{Z_0{}^2 Z_1} \quad ;\ \text{for negative discontinuities.}$$

Since the line is wider than a 50Ω line, we have a negative (or capacitive) discontinuity. Substituting our measured parameters into the second equation above, we calculate $C_{lumped} = 300$ fF. This approximation is valid for all rise times less than the transmission line delay of 11 ps. To model performance above this speed, one should use the full equivalent transmission line. There was excellent agreement between the actual TDR response and the simulated response when using 300 fF lumped elements to model the HYPCON tabs as seen by comparing Figures 4 and 5.

The thru frequency response was also measured using an HP8510 Network Analyzer. The measured response is shown in Figure 6. Two interesting effects are observed: the first is a ripple pattern which grows with increasing frequency, and the second is a 7 dB droop in response at 18 GHz. The ripple component of the frequency response was caused by multiple reflections from

the SMA and HYPCON interfaces, with the amplitude of the ripple controlled by the discontinuity size and the microstrip loss. It was found that the droop component was well modeled with a characteristic skin effect response given by

$$T(f) = 10^{k\sqrt{f}}$$

where $T(f)$ is the circuit transmission as a function of frequency.

To incorporate the measured skin effect into the model, an equivalent circuit proposed by Yen, Fazarinc and Wheeler [4] was used. Each section of microstrip was broken up into 20 sub-sections. Each sub-section was composed of a delay element and a frequency shaping network as shown in Figure 8. An optimizing program [5] was run to determine the best element values to fit both the DC loss and the measured droop for each section of microstrip.

The hybrid trace lines exhibited DC loss. This was caused by the resistance of the traces themselves. Computing the resistance of a 1 inch section of hybrid microstrip agreed with measurements and gave a value of 0.8Ω. This resistance contributes .07 dB loss at DC. The PC microstrip lines had negligible DC loss due to their much larger cross section.

We had considerable difficulty fitting all the details of these measurements. The PC microstrip lines exhibited a change in impedance depending on their orientation. This effect may have been due to non-isotropic plating of the microstrip lines or variation in dielectric constant during manufacture. A few ohms of impedance rise was also seen at the bends in the lines. The size of the HYPCON discontinuity was variable depending on alignment. An attempt was made to model the PC board impedance variation, but the two HYPCON discontinuities were both set to a nominal value.

Several measurements were made to determine the loss of the PC and hybrid microstrip sections. The frequency response measurement was used to determine the overall loss. TDR measurements were then used to help partition the loss between the hybrid and PC lines. The skin loss shows up as a rising slope in the TDR trace. To verify the loss assigned to the hybrid, it was noticed that the magnitude of the ripple pattern observed in the frequency response test was dominated by the two HYPCON discontinuities. These two discontinuities, in conjunction with the loss of the hybrid line, essentially form a Fabry-Perot cavity whose Q is determined by the hybrid loss and the magnitude of the discontinuities. After setting the magnitude of the HYPCON capacitance, it was possible to adjust the hybrid loss until an appropriate amount of ripple was observed. The rest of the loss was then assigned to the PC traces. The value of the PC trace loss was verified by an independent measurement of an isolated section of PC microstrip. The final values for the network are given below in Table 3. The spice model is shown in Figure 9, and the resulting simulated TDR response is shown in Figure 7.

By slicing our model in half, it is possible to predict the one-way performance of the package. Figure 10 shows the frequency response of the package with a 3 dB bandwidth in excess of 11 GHz. Figure 11 shows the response to a 10 Gbit/s data waveform. The package induced risetime degradation is less than 25 ps.

Table 3. Element Values	
Description	Value
SMA interface discontinuity	.108 nH
PC board delay (2.85")	370 ps
PC board loss (6 GHz)	.60 dB
HYPCON tab	300 fF
Hybrid delay (1")	211 ps
Hybrid loss (0 GHz)	.07 dB
Hybrid loss (6 GHz)	.90 dB

5. Conclusions

We have demonstrated a test package with 46 I/O's that allows quick hybrid replacement. The simulated bandwidth is greater than 11 GHz with a package induced risetime degradation of less than 25 ps.

There were several things that we would change in a second pass design. We noticed that the feet of the HYPCON frame have a tendency to smash some of the PC board lines near the screw holes. The affected lines should be moved to avoid the HYPCON footprint. The PC microstrip lines were more lossy than predicted by our microstrip design program. This may have been due to a Nickel layer used between the Copper and Gold layers on the lines. Reduction of this loss could significantly improve the bandwidth of the package.

Because of the large size required to accommodate 46 SMA connectors, this package would not be suitable for use in an instrument. We do believe, however, that the HYPCON should be useful in instrument applications, as demonstrated by Tektronix's use of the HYPCON in its line of sampling scopes.

Overall, we have been pleased with the performance of the package. The HYPCON has proved to be very reliable. Connections are easily made and once made are robust. The frequency and pulse performance are excellent. Along with the electrical properties, we feel that an important contribution has been the reduction of time required to test new high-speed ICs.

References

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