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A 1.5 Gb/s Link Interface Chipset for Computer Data Transmission

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Abstract—**A set of four IC's provide encoding, multiplexing, clock extraction/demultiplexing, and decoding for gigabit-rate serial data transmission. These chips form a high bandwidth data link for point-to-point communication. A new line code is implemented that provides DC balance, efficient encoding, framing, and simple clock extraction. Embedded in the code is a fixed transition used by the phase/frequency locked loop (PLL) for simple clock extraction and frame synchronization. Unlike other links, our PLL requires no trimming for data retiming, either in production or later. An on-chip voltage-controlled oscillator (VCO) with a tuning range of 1.1–1.6 GHz is available for use with the PLL. With this chip set, we have demonstrated a transmission rate of 16 bits in parallel at 75 MHz or, with encoding overhead, a serial rate of 1.5 Gb/s.**

I. Introduction

TELECOM applications have pioneered the use of fiber equipment in voice transmission. Because of the high cost of fiber optic transmitters and receivers, and problems with skew between multiple channels over long distances, serial transmission is generally used for telecom data transmission [1]. However, parallel data interfaces are preferred for convenient connection to computer equipment. The use of fiber media for high-speed computer communication has been limited by the lack of link interface chips required to adapt the parallel format of the computer data into the serial bit streams required for fiber transmission. The link interface chipset must guarantee DC balance of the serialized bit stream (to simplify laser biasing and facilitate receiver design) and provide some scheme for recovering a clock from the data stream. Although there have been several GaAs chipsets published [2], [3] to date, there has been a lack of high-speed silicon bipolar interface chips to provide these functions. The silicon bipolar process is a preferred solution because of its long established reliability record.

We have designed a set of four IC's using silicon bipolar technology for a gigabit rate data link: an encoder chip, a multiplexer (MUX) chip, a PLL chip, and a decoder chip [4]. These chips provide the necessary interface functionality to form a high-bandwidth fiber optic data link for point-to-point communication (Fig. 1). The architecture of the link is largely determined by the line code design which is discussed next.

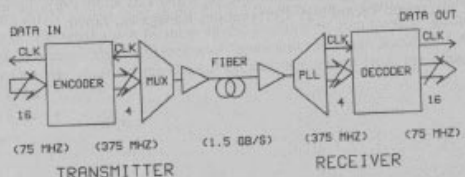

Fig. 1. Block diagram of one half of a duplex link.

II. Line Code, Clock and Frame Synchronization

Coding schemes that satisfy the needs of clock recovery and dc balance are a tradeoff between coder complexity and bandwidth utilization. Simple Manchester coders suffer a bandwidth penalty of 1/2: two symbols are sent for each received bit. Other codes such as 5b/6b [5] and 4b/5b used in FDDI [6] are more bandwidth efficient, but are complex to implement, usually requiring a ROM. By using an efficient code, less raw link bandwidth is required. Our code is only moderately complex to encode, simple to decode, and can be highly efficient [7].

The new code used in this link achieves dc balance by transmitting each M bit data word either inverted or noninverted in such a way that the accumulated offset of the transmitted words is bounded. Only one effective coding bit needs to be prepended to each M bit word to indicate the polarity of the word to the receiver.

We actually use two coding bits rather than one to allow the transmission and recognition of nondata words, such as Fill and Control Words. Fill Words are sent on the link when no data is available, and are discarded by the decoder. Control Words are available for out-of-band signaling.

Finally, two more bits are added which are always "01." This "0" to "1" edge, called the *master transition*, is used by the phase locked loop as the phase reference for both bit and frame clock recovery. The frame clock is used by the PLL demultiplexer for frame alignment. Thus, a total of four extra bits per word are required in this coding scheme for any length of data word. Fig. 2 shows the coding format for a 16 bit data word. Because each frame of the line code incorporates a reference tran-

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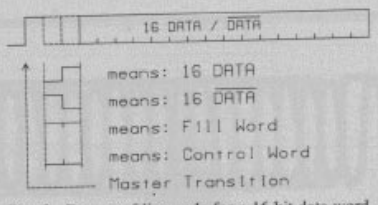

Fig. 2. Format of line code for a 16 bit data word.

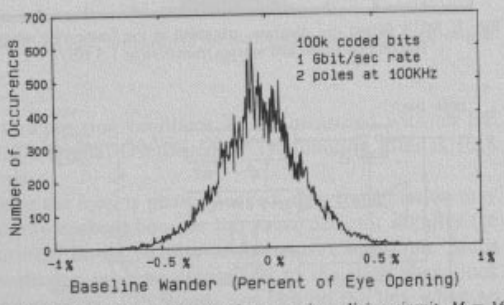

Fig. 3. Histogram of baseline wander at receiver slicing circuit, $M = 16$.

sition, it is not necessary for the user to send any periodic frame-sync words, as is the case with 4b/5b and 8b/10b codes. This allows the link to be conveniently used in a synchronous environment where the insertion of extra frame-sync words is impossible.

Long-term dc balance of the transmitted data permits the regulation of laser bias current by simply maintaining a fixed average optical power. In the receiver, a balanced code permits ac-coupling without eye-degrading baseline wander and jitter.

The dc balance performance of a given code can be characterized by the worst-case long-term disparity of ones and zeroes sent on the link over time. For a code with guaranteed maximum disparity of n bits, transmitted at a data rate R through a channel with k low-pass poles, each with a time constant τ, the percentage peak-to-peak baseline wander at the receiver slicing circuit will be approximately

$$\approx \frac{kn}{2R\tau} \times 100\%.$$

At low data rates R, complex codes with very low disparities n are required to control the baseline wander. At higher data rates, for a given low-pass time constant, longer disparities n are tolerable. This allows a tradeoff of coding complexity and disparity for Gb/s data links.

The dc balance performance of our code can be judged by the baseline wander with two 100 kHz poles in the link; for example, one at the transmitter and one at the receiver. Fig. 3 shows a simulated histogram for 100k bits of random data, coded with $M = 16$, at 1 Gb/s. For these conditions, the baseline wander at the receiver slicing circuit is less than $\pm 1\%$ of the eye opening, corresponding to a maximum accumulated disparity of 24 serial data bits.

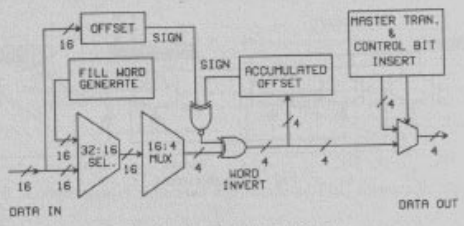

Fig. 4. Encoder block diagram.

III. Encoder Algorithm

A simplified block diagram of the encoder is shown in Fig. 4. As each word enters the encoder, the sign of its offset is detected and compared with the sign of accumulated offset in an XNOR gate. Each nibble of the word is inverted if the signs are the same, and not inverted if the signs are different. The output of the accumulated offset block is updated only at the beginning of each frame so that the invert signal is stable for each of the four data nibbles. The offset of the encoded word is then accumulated nibble by nibble as each nibble is transmitted.

In addition to the sign circuit, there are sections for clock division, Fill/Control Word generation, and serialization. The 4 bit data path is pipelined to provide minimum delay between stages, operating with a 2.5 ns minimum cycle time. Input and output latches are used to provide maximum timing margin for external connection of the chips.

The hardware for encoding of the data is simple, consisting of exclusive-OR gates.

A. Sign Circuit

An analog circuit, corresponding to the "offset" block in Fig. 4, was implemented to determine the sign of the offset of a 16 bit word (Fig. 5), i.e., whether it has more ones or zeroes. Sixteen current switches, one for each bit, steer a unit current into one of two summing resistors, generating a differential voltage proportional to the difference between 1-bits and 0-bits. A comparator detects the polarity of the voltage, giving the sign of the word. An extra current source shifts the threshold from the balanced condition so that a word with eight ones and eight zeroes will produce a known sign.

This embedding of an analog circuit in an all-digital chip gives a faster, lower power implementation. The requirement for matching of current sources is tighter than for the logic gates but is still within the capabilities of a conventional digital bipolar process.

B. Accumulator

In a simple-minded approach to the accumulator, the serialized bit stream could be applied to an up/down counter: counting up for ones and down for zeroes. The MSB of the counter would give the sign of the accumulated offset. Since the feedback forces the offset toward zero, the required size of the counter is bounded: it is

in transient can be simulated on an HP 9000/350 UNIX workstation in about 3 min of real time.

VI. Decoder Chip

The decoder provides the companion functions of deserialization and decoding. A block diagram is shown in Fig. 11. No processing is done on the frame until it is in full parallel form. A framing pulse generated in the phase locked loop synchronizes the clock divider phase to the incoming frame and correctly aligns the demultiplexer. If the frame contains data, the added coding bits are used to enable or disable the word inverter. If the word is a Fill or Control Word, it is identified and decoded. Like the encoder, all data inputs and outputs are latched.

VII. Link Startup and Maintenance

Some of the nondata codes are used during link setup. An end-to-end handshake ensures that both ends of a full duplex link are frequency and phase locked before data is transmitted.

Fig. 12 is a state diagram describing the startup handshake procedure for a full duplex link. Both the near and far ends of the link independently follow the state diagram of Fig. 12. At power up, each end of the link enters the sequence at the arc marked "START."

Each node in the state machine has three notations. The top notation is either "FDET" or "PHASE." FDET stands for frequency detect mode, and implies that the frequency detector has been enabled on the PLL chip. When the chip is in this mode, it is important that no data is being sent, as the frequency detector is only able to lock onto one of the special training Fill Words: FW0 or FW1. The PHASE notation means that the PLL has been switched to phase detect mode and is ready to allow data transmission. The middle notation in each state bubble is the Fill Word which is currently being sent by the node's encoder and MUX. The last notation is the ready for data (RFD) status on the encoder chip. When RFD is low, the encoder signals the user to hold off any incoming data while it sends Fill Words. When RFD is high, data is sent if available; otherwise Fill Words are sent.

The consistent presence of the two *master transition* bits is monitored by the decoder chip to detect a locked condition. If the decoder detects an unlocked condition, then this is flagged to the startup state machine as a frame error. The decoder chips at both ends of the link are able to detect four different conditions: frame error (FE), data (DATA), Fill Word 0 (FW0), and Fill Word 1 (FW1). Transitions are made from each of the states based on the current status condition received by the decoder. Each of the subsequent arcs in the diagram are labeled with the relevant state that would cause a transition along that arc.

It is worth noting that if either side of the full duplex link detects a frame error, it will notify the other side by sending FW0. When either side receives FW0, it follows the state machine arcs and reinitiates the handshake. The user is notified of this action by the deasserting of the RFD signal.

This startup protocol provides the user with a guarantee that no data will be accepted until the link is able to deliver data. The use of a training sequence handshake avoids any false lock problems inherent in PLL systems which attempt to lock onto random data with wide-range VCO's.

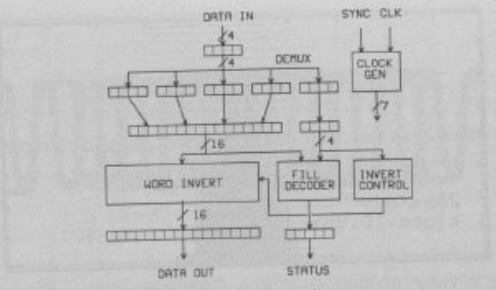

Fig. 11. Decoder block diagram.

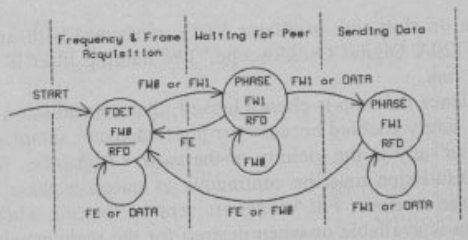

Fig. 12. Link startup procedure.

TABLE I
Chipset Overview

Chip	Function	Size (mm)	Power
Encoder	Encoding 16:4 multiplex	4 × 5	3 W
MUX	4:1 multiplex	1.3 × 2	1 W
PLL	Clock recovery 1:4 demultiplex	2.3 × 2.6	1.5 W
Decoder	Decoding 4:16 demultiplex	4 × 4	2 W

VIII. Implementation

An overview of the four chips described is given in Table I. The encoder and decoder chips are fabricated in a 5 GHz f_t bipolar process, using emitter function logic [12] standard cells. They contain 2500 and 2000 active devices, respectively. Packaged parts run up to 400 MHz, capable of supporting a serialized line rate of 1.6 Gb/s. The MUX and PLL chips are implemented in a 10 GHz f_t bipolar process using full custom ECL design. They contain 350 and 950 active devices, respectively. A pc board containing all four chips has been developed, and link speeds of 1.5 Gb/s have been demonstrated.

ACKNOWLEDGMENT

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