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TPM 8.7: A Monolithic 622Mb/s Clock Extraction Data Retiming Circuit

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In high-speed digital transmission systems, a digital waveform must be regenerated to insure data integrity. This is usually done by extracting a clock directly from the input data stream using a non-linear function with a band-pass filter, and then using this clock to trigger a decision circuit which reshapes the data stream. The band-pass filter is typically a SAW filter or PLL. This method is accepted as the norm for systems above 200Mb/s. However, the design of such a system requires careful alignment of the data relative to the clock over temperature, supply variation, process variations, and age. Also, this approach is relatively expensive since the components are difficult to integrate.

In this report, an architecture based on a different technique is described. This retiming circuit incorporates all the functions of clock recovery, data regeneration, and clock to data alignment. Except for two external capacitors, the circuit is fully integrated. The targeted bit rate is centered at 622.08Mb/s, the standard rate for SONET OC-12.

The overall circuit is comprised of three main blocks, as shown in Figure 1. The first block is a phase/frequency detector, which compares NRZ data to the clock, and produces a binary output. In addition, a built-in decision circuit retimes the data in the center of the data eye. The second block is a charge pump which integrates the detector output. The clock is generated by the third block, a special VCO with one input which sets the center frequency, and another which toggles the VCO between two small but discrete frequency offsets. The output of the detector directly controls the toggling. The integrator output sets the center frequency of the VCO.

The block diagram of the detector is shown in Figure 2. This phase detector is similar to one proposed by Alexander.[1] The input is first split by a low-noise amplifier into flip-flops **B** & **T**. The output of **B** feeds flip-flop **A**. Both **A** & **B** are toggled by CLK, while **T** is toggled by $\overline{\text{CLK}}$. This results in the sampling of the input data at three distinct points; prior to, in the vicinity of, and following each potential transition. If a transition is present, the phase relationship of the data and the clock can be deduced to be fast or slow. The phase detector output is combined with that of a frequency detector, which yields the final detector output. Note that under locked conditions, **T** is always at the edge of the data eye, and that flip-flops **A** & **B** are always sampling the center of the data eye. Therefore, the output of flip flop **A** could be used as the retimed data output, emulating the function of a decision circuit.

The VCO is designed with a ring oscillator, as shown in Figure 3.[2] This ring consists of three variable-delay cells plus a bang-bang delay cell which has an additional small delay inserted on command. The variable delay cell is a continuous interpolation between two cells of different delays. The analog inputs to these cells form the center frequency control for the VCO. The bang-bang delay cell is designed with three sections. The digital input is sliced down to a lower level. This voltage is then converted into current with a transconductance cell, which modulates the bias current of buffer biased below the peak f_T current.

The overall ring is designed to have a nominal delay of about 800ps, corresponding to 622MHz, with an extended range of ±20%. The bang-bang time is about 3ps. The response time of the bang-bang modulation is within 700ps, much less than one clock cycle at 622 Mb/s.

The circuit was laid out using a quick-turnaround prototyping and production tool for gigahertz ICs and was fabricated using the a silicon bipolar process with a 10GHz peak f_T.[3] The chip measures 2.8x2.8mm, and is mounted in a microwave surface-mount package.[4] External 39nF monoblock capacitors are used for the integrator and supply bypassing. Die and package photos are shown in Figure 4.

With V_{EE} = -5.2V and V_{TT} = -2.0V, the total power dissipation is 1.25W. With a PRBS=(2^{23}-1) input at 622Mb/s, the acquisition of the retiming circuit is measured with a time frequency analyzer as shown in Figure 5. The VCO starts at its upper frequency and acquires lock in less than 1ms. The eye diagrams of the input and regenerated output, as well as the recovered clock, are shown in Figure 6. The jitter of the recovered data measured at the eye crossing is shown in Figure 7. The measured rms jitter generated by the bang-bang is 7.4ps, which is less than 0.5% of the eye at 622Mb/s. An integrated clock extraction data retiming circuit operating at 622Mb/s has advantages over traditional designs: tolerance to environmental variations, autocentering of the clock to the input eye, and the lack of adjustments in production. The level of integration also yields the benefits of reduction in size, improved reliability, and the potential for major cost reduction. This architecture can be extended to other bit rates.

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[1]Alexander, J. D. H., "Clock Recovery from Random Binary Signals", IEEE Electrons Letters, vol 11, pp. 541-542, October 1975

[2]Walker, R. C., "A Fully Integrated High-Speed Voltage Controlled Ring Oscillator", November 1989. U.S. Patent Number 4884041.

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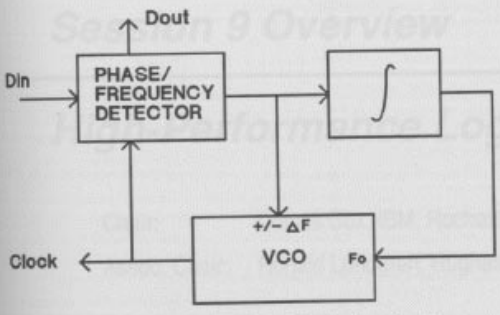

Figure 1: Block diagram of retiming circuit

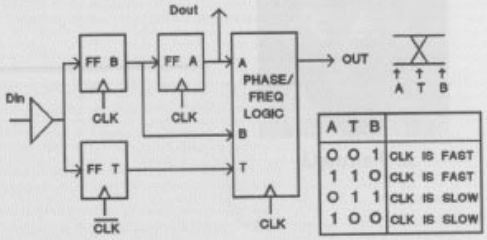

Figure 2: Block diagram of phase/frequency detector

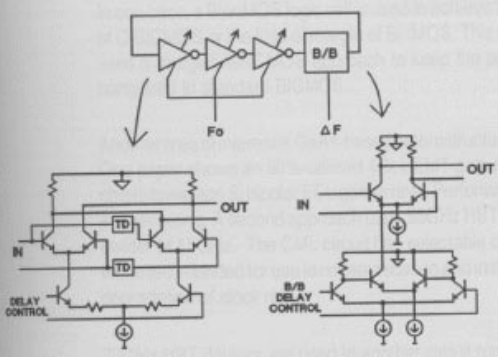

Figure 3: Voltage-controlled ring oscillator

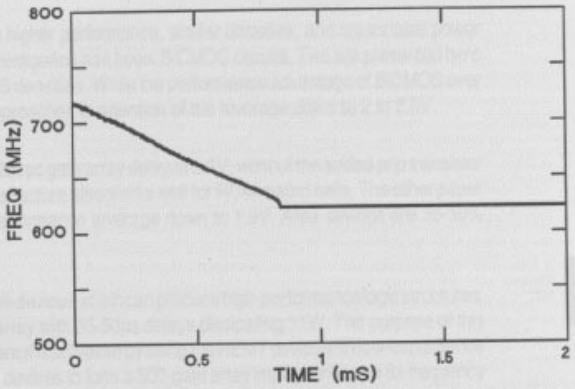

Figure 5: Measured acquisition of retiming circuit

FIGURE 5 — *See page 306*

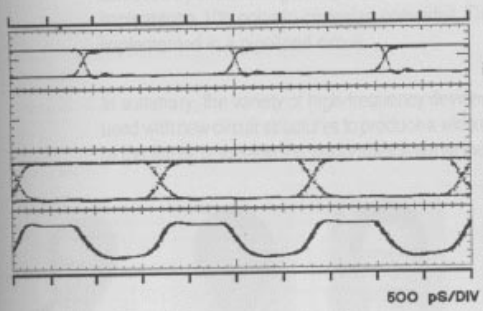

Figure 6: Eye diagrams of input & output, and extracted clock

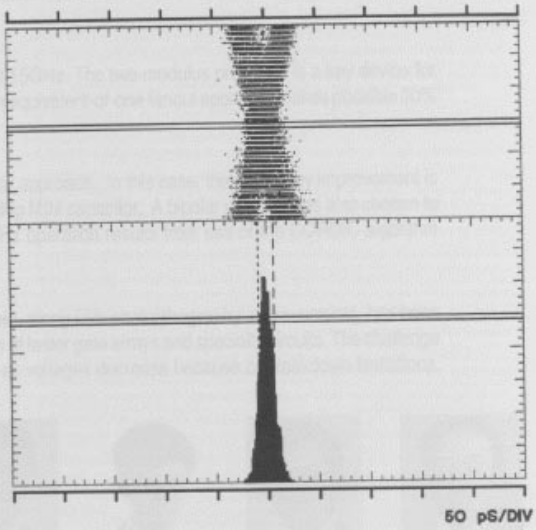

Figure 7: Jitter histogram of regenerated data