A GENERAL-PURPOSE LINK INTERFACE CHIPSET FOR GIGABIT RATE DATA COMMUNICATION

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ABSTRACT A chipset has been developed for transmitting parallel data over serial links. The chipset, consisting of a Transmitter Interface Chip (TIC) and a Receiver Interface Chip (RIC), can support serial transmission up to 1.4 Gbaud. Data encoding is based on a scheme published early, but has been improved to provide more flexibility and better efficiency. The new chipset requires no other external components for its operation except for only a few capacitors, which are built into its custom package.

I. INTRODUCTION

Use of gigabit rate optical links has not been widespread because of the lack of low cost, easy-to-use, link interface chips. Functions required for these high speed chips include parallel-to-serial and serial-to-parallel conversions, data encoding and decoding, clock generation and clock recovery.

We have developed a chipset capable of handling gigabit rate data. The chipset, made in silicon bipolar process, consists of 2 chips: a Transmitter Interface Chip (TIC) and a Receiver Interface Chip (RIC). These chips provide all the necessary functions for transmitting parallel data over serial links. Fig. 1 shows a duplex optical link for gigabit rate computer interconnect.

II. THE G-LINK CHIPSET

The chipset is known as the Hewlett-Packard G-link Chipset [1]. Fig. 2 shows the Transmitter Interface Chip. It contains 6000 active devices, and dissipates about 2 W. Fig. 3 shows the Receiver Interface Chip. It contains 6600 active devices, and dissipates about 2.5 W.

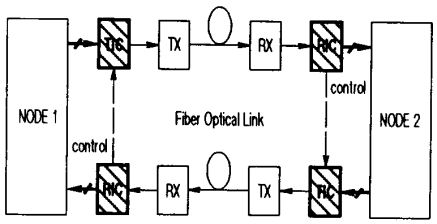

Fig. 1. Duplex Optical Link

The chipset can work with either 16-bit or 20-bit wide parallel data. An optional flag bit is also available, which can be used as the 17th or 21st bit.

The on-chip high speed TIC clock is phase locked to the input word clock supplied by the user. As an option, a clock at one half the required rate is also acceptable. This is found to be very convenient for applications like Serial HIPPI [2]. The chipset can operate at 1/2, 1/4, or 1/8 of the designed serial rate, allowing operations from 120 Mbaud to 1.4 Gbaud in four bands.

For short distances, the chipset can be used to drive coaxial cables directly. An optional on-chip cable equalizer is provided in the RIC. It can extend the maximum length of some of the commonly used coaxial cables by as much as 50%.

Additional serial loopback output and input are provided by the chipset for fault isolation.

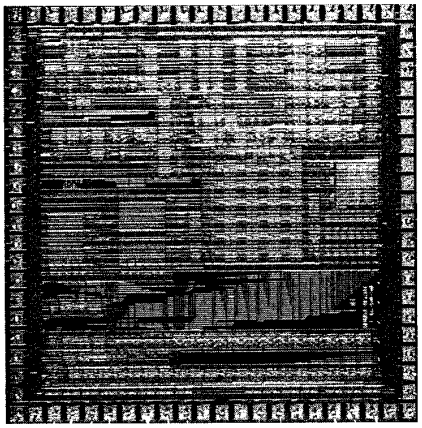

Fig. 2. Transmitter Interface Chip, 3.4x3.4 mm

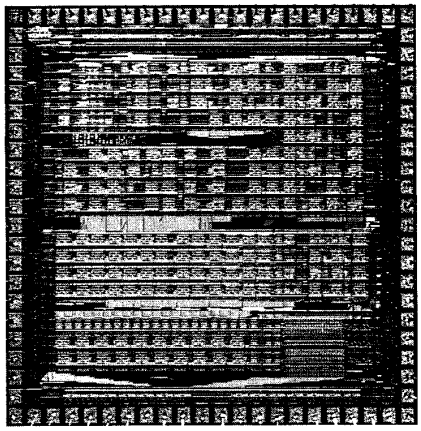

Fig. 3. Receiver Interface Chip, 3.4x3.4 mm

III. LINE CODE

The code used in the G-link chipset achieves DC balance by transmitting the input data either inverted or non-inverted (true). The selection is based on which will result in a smaller accumulated offset of the transmitted frames. To carry this and other coding information, four bits are appended to the input data to form a Data frame as shown in Fig. 4, 20-bit frames for the 16-bit mode, 24-bit for the 20-bit mode. The code also support the transmission and recognition of two kinds of non-data frames: Fill frames and Control frames. The former are sent on the link for startup synchronization, and for maintaining synchronization when no other frames are sent. The latter are provided for link maintenance. The allowed number of Control frames is extensive in this design: 2^14 for the 16-bit mode, and 2^18 for the 20-bit mode.

Master transition is an integral part of this code. Unlike the early reported version [3] where the two bits bracketing the master transition are always "01". The new design allows both "01" and "10" when transmitting data. This is controlled by a flag input, which is made available to the user as an extra input bit. This extra bit proves to be a very useful feature in some application[2,4]. It also improves the coding efficiency by a few percent.

The master transition is used by the phase-locked loop as a phase reference for clock recovery. It is also used as a reference for frame synchronization.

For the past few years, this coding scheme has been known as the HP 16B/20B or 20B/24B code, depending on the data width. When the flag bit is included, it is sometimes referred to as the 17B/20B, or 21B/24B code. A better descriptive name is "Conditional Inversion with Master Transition", or the CIMT code, which avoids explicit reference to the data width.

Flag	Data Field	Code Field
0	True	1 1 ¦ 0 1
0	Inverted	0 0 ¦ 1 0
1	True	1 0 ¦ 1 1
1	Inverted	0 1 ¦ 0 0

Master Transition

Fig. 4. 20/24 bit Data Frame

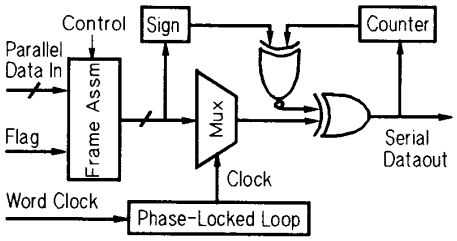

Fig. 5. Simplified TIC Block Diagram

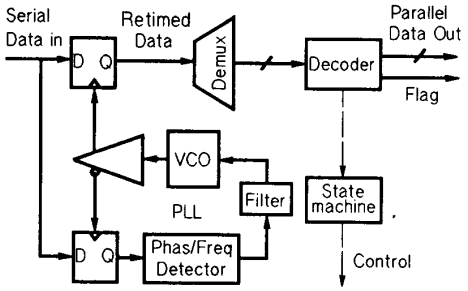

Fig. 6. Simplified RIC Block Diagram

IV. TRANSMITTER INTERFACE CHIP (TIC)

A simplified block diagram of the TIC is shown in Fig. 5. The combination of the XNOR and the XOR gates constitutes the Conditional Inversion part of the encoder. The sign circuit determines the offset of the input frame, (i.e., whether it has more "1"s than "0"s), and the up/down counter determines the accumulated offset of the transmitted frames. The outputs of these two circuits determine whether the incoming frame is to be inverted or not.

The TIC also contains circuits for frame assembly, parallel-to-serial conversion (Mux), and clock generation. The phase-locked loop used in the TIC is similar in design to that in the RIC. They use the same VCO design in order to maintain the same operating frequency range.

V. RECEIVER INTERFACE CHIP (RIC)

Fig. 6 is a simplified block diagram of the RIC. The input serial data is sampled by two D-latches, each is clocked by one of the two complementary outputs of a differential driver. When the clock of the lower D-latch is phase locked to the master transition, the upper D-latch samples the data exactly at the center of the bit. This relationship is maintained because the clock signals are complementary to each other and the two latches are matched pairs. No adjustment is required for data retiming.

Serial-to-parallel conversion is performed by the demux circuit.

Decoding is extremely simple. Depending on the information carried by the four coding bits, the data field is either inverted or non-inverted.

VI. LINK SYNCHRONIZATION

A state machine is included in the RIC, Fig. 6, for initiating end-to-end handshake to ensure that both sides of a full duplex link are frequency and phase locked before data is allowed to transmit.

Synchronization between the TIC and the RIC is achieved by sending special Fill frames as training sequences. Fill frames contain only a single rising edge per frame, which is the Master Transition. Initially the phase/frequency detector works as a frequency detector. when the VCO frequency is brought to within the pull-in range of the loop, the phase/frequency detector operates as a phase detector. Once the loop is phase locked, transmission of Data or Control frames can begin. To keep the phase-locked loop operating, the RIC must receive one of the three types of frames at all time.

The four coding bits are monitored continuousely for the presence of the master transition and the valid coding states. Persistent violation is interpreted as loss of lock, and an automatic restart will be initiated by the state machine.

VII. SUMMARY

A link interface chipset using silicon bipolar process has been developed. Features of this design includes high speed (up to 1.4 Gbaud), single power supply, low power dissipation, ease of use, and low cost. The simplicity of the CIMT coding scheme is directly responsible for the small size of the G-Link chipset.

The chipset has been accepted by Serial HIPPI [2], an ad hoc implementor's group, and by SCI, an IEEE P1596 standard [4]. The many features provided in this chipset should make it an ideal choice for gigabit rate data communication.

References:

[1]. "The G-Link Interface Chipset", Hewlett-Packard Co., V.1.02, February 1992.

[2]. "Serial-HIPPI Specification", Rev. 1.0, Serial HIPPI Implementors Group, May 17, 1991.

[3]. R. C. Walker, et al. "A 1.5 Gb/s Link Interface Chipset for Computer Data Transmission", IEEE Journal on Selected Areas in Communication, vol. 9, no. 5, June 1991.

[4]. "SCI - Scalable Coherent Interface, P1596/D2.00", Draft for Recirculation to the Balloting Body, November 1991.