A Bipolar 1.5 Gb/s Monolithic Phase-Locked Loop for Clock and Data Extraction

Jieh-Tsorng Wu

Microwave Semiconductor Division
Hewlett-Packard Company
San Jose, California 95131

Richard C. Walker

Laboratories
Hewlett-Packard Company
Palo Alto, California 94303

Abstract – **This paper describes the design of a monolithic phase-locked loop (PLL) used in a gigabit serial data link interface [1] for clock and data extraction. Implemented in a triple-metal 25 GHz f_t bipolar process and consuming 85 mA from a 5 V supply, the PLL has a wide frequency acquisition range, from 600 MHz to 1.5 GHz, and a recovered clock phase jitter less than 18.3 psec rms. The PLL requires only one external component which is the loop filter capacitor, needs no adjustment, and is suitable for large-scale integration.**

Clock recovery and data extraction are the crucial functions in high-speed base-band digital communication systems, such as optical fiber channels. Extraction schemes based on PLL's have become attractive because of their suitability for integration. By employing a line code that is conscious to synchronization, the PLL described here achieves robust performance with efficient design.

The PLL functional block diagram and the input line code is shown in Figure 1. The line code is a consecutive sequence of data frames. Each data frame has six nibbles, and each nibble has four non-return-to-zero bits. A *master transition* is always presented at the center of the sixth nibble. During link start-up, the remote transmitter sends a series of fill words, which create a square wave that has its rising edges at the master transition location. The receiver uses the fill words as a training sequence to acquire clock frequency and to align the internal Sync Ref clock with the master transition. For regular data frames, the PLL detects only the phase difference between the Sync Ref and master transitions, while ignoring all other transitions. The divide-by-N divider shown in Figure 1 illustrates that the Sync Ref has the same frequency as the data frame. The PLL's phase-frequency detector has only one output – PHI. It has a binary value and stays constant until the next Sync Ref cycle. The VCO has two separate inputs. Its wide-range tuning frequency, f_{tu}, is controlled by PHI filtered by a single-pole low-pass filter. The other input is directly driven by PHI and produce a tiny VCO frequency deviation, called the bang-bang frequency ($\pm f_{bb}$), from the tuning frequency.

The input sampler shown in Figure 2 extracts both data and phase information from the serial input. The *data sampler* (LAT1–LAT3) and the *phase sampler* (LAT4–LAT5) are implemented with identical regenerative latches to minimize phase offset. The PLL adjusts its VCO phase so that the phase sampler samples the serial input at the data bit boundary. Assuming a 50% duty cycle VCO clock, the data sampler then samples at the center of the data bit. The enabled flip-flops (FF1–FF5) are used to select the sampled output at a given position in a data frame. The enable signals are decoded from a ring counter that circulates once per frame. For example, the MT signal is the phase sampler output at the master transition, and the PF signal is the data sampler output one half bit period before the master transition. During normal operation, the phase-frequency detector output PHI is the exclusive-OR of MT and PF.

The phase-frequency detector circuit schematic is shown in Figure 3. Note the the signal PF is omitted for simplicity. During the training phase of the link, the remote transmitter sends out fill words, and the receiver enables the frequency detector by setting FDIS=0. The frequency detector is a classical sequential detector, which consists of FF1, FF2, and AND1. The flip-flop FF3 is added to latch the sequential detector's output. Because the phase alignment of the frequency detector is not accurate, when the phase of Sync Ref is within approximately ±45 degree of the master transition, the PLL switches to the MT phase sampler for final phase adjustment. This is automatically achieved with additional samplers, BF1, BF2, BF3, and AND2. The signals MT and BF1–BF3 all come from the input phase sampler. With the equally-spaced phase sampling locations shown in Figure 3, when all three outputs from BF1–BF3 are low, PHI selects the output from the MT sampler. The frequency discrimination range is greatly enhanced by gating the phase detector output with the three BF samplers rather than one alone. Once the PLL is phase-locked, the MT sampling occurs at the master transition, and the MT sampler is always selected to the PHI output. The frequency detector must be disabled (by setting FDIS=1) during regular data frame transmission.

The PLL is monolithically integrated in a receiver chip. Its signal paths are fully differential to maximize noise immunity. Current sources are biased with the band-gap reference shown in Figure 4. The compensation circuitry that consists of Q11–Q13 and associated components is added to reduce the V_{CS} sensitivity to V_{EE} variation. The VCO is a ring oscillator consisting of three identical variable-delay cells [1]. The VCO has a continuous tuning range

92CH3173-2/92/0000-0070$3.00 © 1992 IEEE

from 600 MHz to 1.5 GHz. The PLL loop filter is shown in Figure 5. The external capacitor C1 is placed inside the package to reduce parasitic inductance. The positive feedback path (Q5, Q6, and R3) is used to boost the effective resistance of R1 and R2, making the filter function more like an integrator.

When locked, the measured VCO phase jitter is shown in Figure 6. The phase jitter varies at different locations within the data frame. The maximum jitter is 18.3 psec rms which occurs at the frame boundary (0 degree), while the minimum jitter is 9.7 psec rms at the frame center (180 degree). The input phase jitter is 3.7 psec rms; thus, the jitter shown in Figure 6 is dominated by the bang-bang frequency hopping.

ACKNOWLEDGMENTS

The authors would like to thank C. Stout, B. Lai, C. Yen, T. Hornak, and P. Petruno.

REFERENCES

[1] R. Walker, J.-T. Wu, C. Stout, B. Lai, C. Yen, T. Hornak, and P. Petruno, "A 2-chip 1.5 Gb/s bus-oriented serial link interface," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, FA14.4, February 1992, in press.

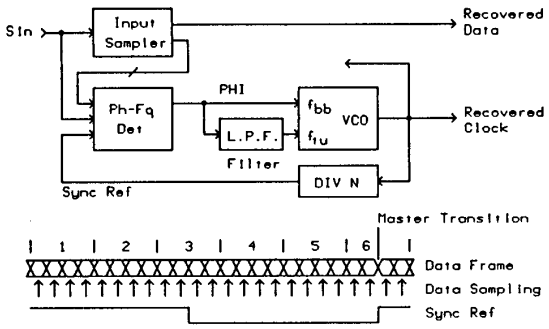

Figure 1: Phase-locked loop functional block diagram.

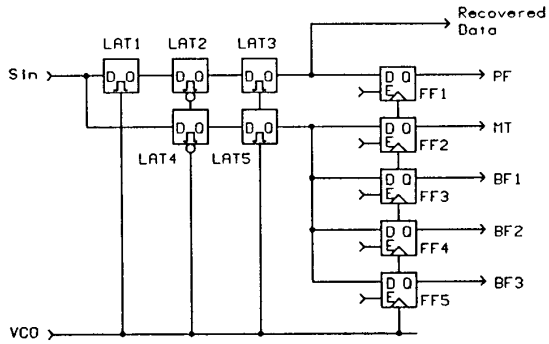

Figure 2: Front-end input sampler circuit schematic.

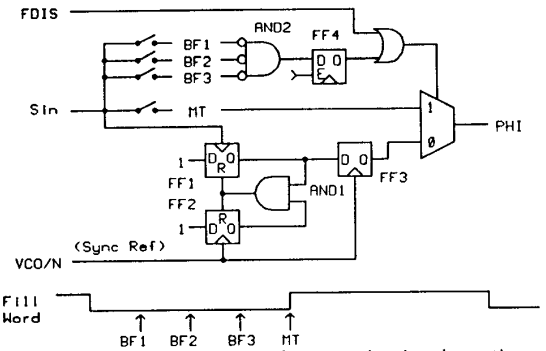

Figure 3: Phase-frequency detector circuit schematic.

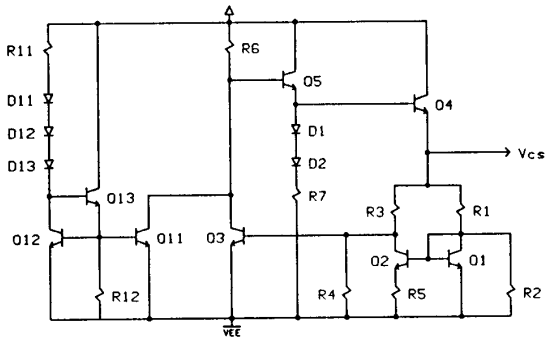

Figure 4: Band-gap reference circuit schematic.

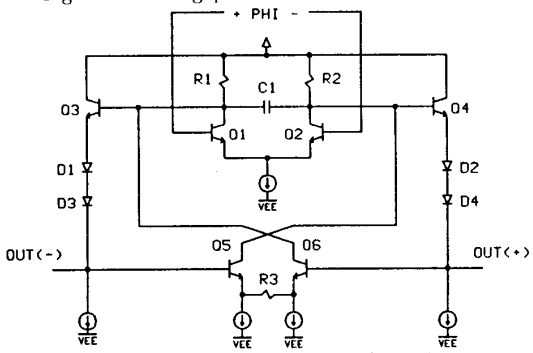

Figure 5: Loop filter circuit schematic.

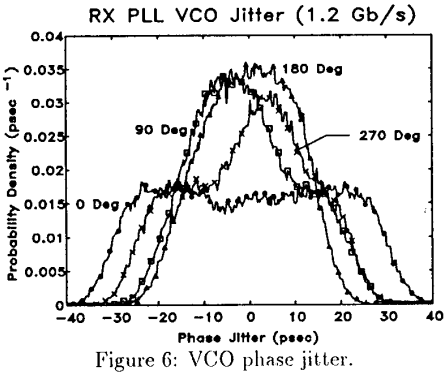

Figure 6: VCO phase jitter.