## FA 14.4 A 2-Chip 1.5Gb/s Bus-Oriented Serial Link Interface

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Parallel computers, high-resolution graphics and network backbones are among the many application areas that could immediately benefit from inexpensive, compact, easy-to-use gigabit-rate data links. An earlier 4-chip chipset established the feasibility of several integrable circuit techniques to achieve these data rates, but was difficult to use because of the high-speed chip interconnections and extra support circuitry required [1]. The monolithic transmitter (TX) and receiver (RX) chip pair reported here implement a full-duplex "virtual ribbon cable" interface (Figure 1). For short-distance applications, an on-chip equalizer is provided to allow use of coaxial cables rather than a more costly fiber link. The chips require no external frequency-determining elements or user adjustments and operate over a range of 600 to 1500MHz using an on-chip VCO. Only one in-package capacitor per chip is required. A state-machine controller (SMC) is also implemented on the RX chip to transparently handle a start-up handshake protocol. This is the highest-speed link-interface chipset reported to date at this level of functionality and integration.

A simplified block diagram of the TX chip is shown in Figure 2. The PLL/clock generator block generates the high-speed serial clock by phase-locking onto the incoming low-speed clock, which can be either at the full- or half-frame rate. A programmable option allows the TX chip to accept either 16b or 20b of data to produce a 20b or 24b line code frame. In addition, an extra input FLAG bit is also available that can be used either as an extra data bit, thereby transmitting 17b or 21b of user data, or can be internally toggled by the transmitter to allow enhanced receiver frame error detection.

To implement the line code, the parallel data words are transmitted in either true or complement form, as needed, to maintain dc balance on the line (Figure 3). To make the decision, the TX chip uses a DAC to compute the polarity of the incoming word and compares it to the sign of an up/down counter which keeps track of the total disparity of transmitted bits. If the two signs agree, the word is sent inverted. Otherwise it is sent uninverted. 4 extra coding bits (C-Field) are appended to the data field (D-Field) during transmission. The central pair of bits in the C-Field are always complementary and provide a "master transition" phase reference for the receiver PLL. The polarity of this master transition is used to encode the extra FLAG bit. The other two bits in the C-Field are used to signal whether a given frame represents inverted data, non-inverted data, inverted control, non-inverted control, or fill. Control frames are special non-data frames that can be used as packet headers, trailers and other protocol-specific information. Fill frames have only a single rising edge at the master transition location, and are used as training sequences to provide unambiguous frequency, phase, and frame acquisition during link start-up. The 17b form of the line code is accepted as the standard code for the IEEE P-1596 Scalable Coherent Interface (SCI) Group, and the 21b form of the code is accepted by the Ad-Hoc High Performance Parallel Interface (HIPPI) Serial Implementors Group.

A simplified block diagram of the receiver is shown in Figure 4. The data path consists of an input selector, two input sampling latches, a demultiplexer, a control-field decoder, and a data-field decoder. The input selector allows either a normal data input (DIN), a loopback data input (LIN) or an equalized input (EQIN) to be chosen at user command. The equalized input implements a shelf filter providing a 3db boost at 600MHz to compensate for skin-loss in long coaxial lines [2]. The improvement of link BER with the equalizer is shown in Figure 5. For a given BER, the equalizer extends the usable link length by over 50%.

An on-chip PLL is used to extract a timing reference from the serial input. The incoming data stream is latched on both the rising and falling edges of the bit-rate VCO clock. When the loop is locked, the rising-edge latch samples the center of each data bit and produces retimed data. The falling-edge latch samples the transitions between bits. The sample corresponding to the master transition is corrected for transition polarity by being XORed with the immediately-preceding data bit to derive a binary-quantized (bang-bang) phase error indication. Because the phase detector and retiming latches are matched, assuming a 50% duty cycle VCO, the retiming clock phase is inherently aligned within the bit cell over both process and temperature variation. With a low-jitter input, the RX recovered clock jitter is below 19ps rms.

The VCO is composed of a cascade of 3 variable delay blocks as shown in Figure 6. The main tuning input is bandwidth limited to reduce its sensitivity to on-chip noise, and tunes over a 500-1600MHz range by interpolating between delay gates. The bang-bang tuning input has a wide tuning bandwidth, but only produces a ±0.1% variation in VCO center frequency by modulating the base charge in Q1 and Q2.

The SMC controls the TX and RX chips during link startup, and detects error conditions when they arise. For fiber applications, the SMC can also provide laser eye-safety, with the addition of an external timer and an OR gate, by pulsing the laser at a low duty-cycle when a fiber is broken.

The two chips are implemented in a 3-level metal, 25GHz $f_T$, silicon bipolar process using full-custom differential 4.5V ECL design [3]. Both chips with their bypass and integrating capacitors are housed in a custom 68-pin surface-mount package. The 1.8W TX and 2.0W RX chips are both 3.5x3.5mm$^2$ and utilize 6100 and 6600 active devices, respectively. Both chips were fully functional at first silicon. Figures 7 and 8 show micrographs.

*Acknowledgments*

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*References*

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[2] Yen, C-S., and R. Crawford, "Distribution and Equalization of Signals on Coaxial Cables Used in 10Mbit/s Baseband Local Area Networks". IEEE Trans. on Communications, COM-31, 10, Oct. 1983.

[3] Huang, W. M., et al., "A High-Speed Bipolar Technology Featuring Self-Aligned Single-Poly Base and Sub-Micron Emitter Contacts," IEEE Electron Device Letters, vol. 11, no. 9, pp. 412-414, Sept. 1990.

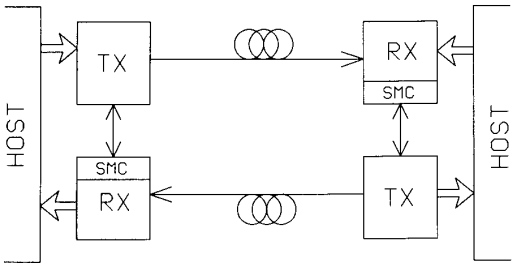



Figure 1. Block diagram of full-duplex link built from 2 chipset pairs.

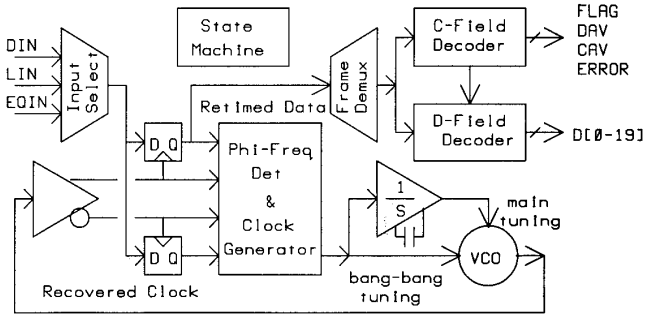



Figure 4. Simplified RX chip block diagram.

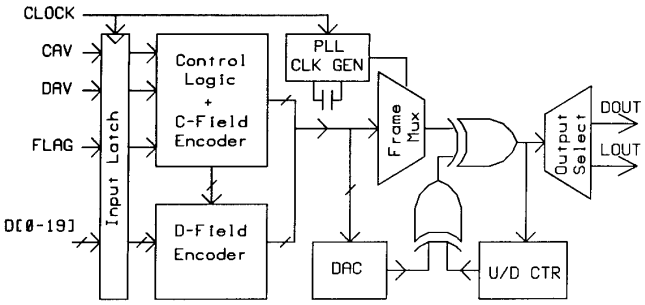



Figure 2. Simplified TX chip block diagram.

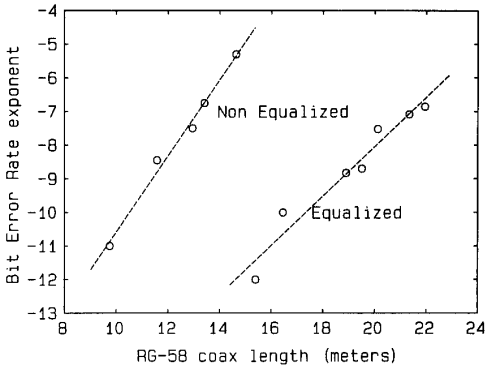
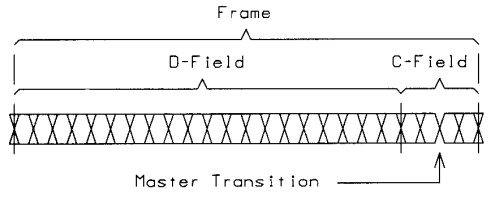



Figure 5. Link BER vs. distance of RG-58A/U coax w/wo equalizing amplifier.




| C-Field | D-Field | Flag Bit |
|---|---|---|
| 1 1 0 1 | True | 0 |
| 0 0 1 0 | Inverted | 0 |
| 1 0 1 1 | True | 1 |
| 0 1 0 0 | Inverted | 1 |

Figure 3. 21b (20+Flag) form of line code frame structure.

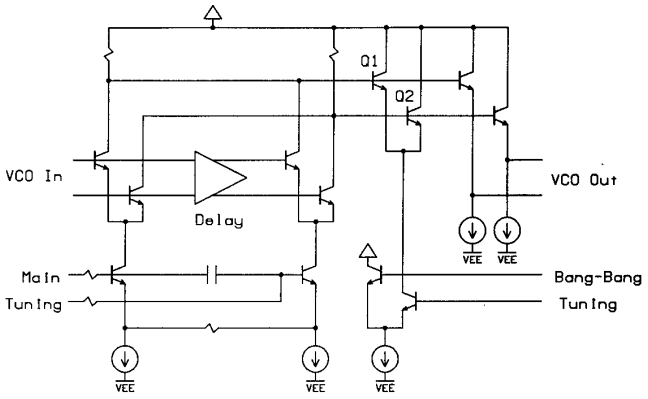



Figure 6. Variable delay block used in ring oscillator VCO.

Figure 7: See Page 291.
Figure 8: See page 291.