TP 9.1: A 16-PSK Modulator with Phase Error Correction

Bernd Wüppermann, Brian Fox, Rick Walker[1], Simon Atkinson[2], Dan Budin[3], Colin Lanzl[3], Scott Bleiweiss[3]

Hewlett-Packard Bipolar Business Unit, Santa Clara/[1]Hewlett-Packard Laboratories, Palo Alto, CA/[2]Mosaic Microsystems Ltd., West Malling, England/ [3]Windata Co., Northboro, MA

Wireless communication systems, such as WLANs and wireless PBX, are moving from the prototype stage to mass production. For high-data-rate applications, e.g. wireless computer links for a large number of users or video links, a modulation scheme with high spectral efficiency (S_e) is desirable. In the future, PSK systems will move from the traditional BPSK and QPSK ($S_e \leq 2$b/s/Hz) modulation schemes to 8, 16-PSK ($S_e \leq 4$b/s/Hz) or even higher level PSK or QAM systems [1,2].

The monolithic integrated transmitter (Tx) reported here is part of a 3-IF-chip set for a 16-PSK transceiver. The other two chips are a fully-integrated quadrature IF-to-baseband down converter and a dual-conversion 5b analog-to-digital converter (ADC). The Tx converts a 4b digital input data word into a defined phase state of the IF. A first-order error correction results in a maximum absolute phase error of less than 1.5° at an IF of up to 400MHz, without external adjustments.

Figure 1 shows a simplified block diagram of the 16-PSK modulator. The input decoder translates a 4b data word into two 4b I and Q data words which switch the following digital to analog converters (DAC). The input code 0000 corresponds to 0° IF phase shift, 0001 to 22.5°, ..., and 1111 to 337.5°. The two mixers generate the in-phase and quadrature vector components that are combined for the desired phase state of the IF. The following 4b digitally-controlled amplifier (DCA) is logarithmic with gain variable in 5dB steps. This enables output power control over a dynamic range of 70dB. The differential output amplifier can be turned off by a single switch (squelch). The maximum IF output power of the modulator is 4dBm. Linearity is maintained throughout the IF path. The voltage-controlled oscillator (VCO), the variable divider, the digital tri-state phase-frequency detector (PFD) and the loop amplifier are building blocks of a phase-locked loop (PLL). For a low phase error, accurate in-phase and quadrature (I/Q) generation is essential. There are two standard methods to obtain a highly accurate on-chip 90° phase shift of a sinusoidal signal: 1) with a frequency doubler and a divide-by-four (a divide-by-two would be duty-cycle sensitive), 2) with a delay locked loop (DLL). Solution one has the disadvantage that the VCO has to run at two times the IF frequency. As a result, the external tank circuit is more sensitive to package parasitics. The DLL solution consumes more power but is chosen so a simple and cheap plastic package can be used for the chip, despite considerable package parasitics (Figure 2). The DLL operates by sensing the I/Q phase difference with an XOR phase detector. A summer and a limiter use the integrated phase difference to modulate the clock pulse-width of a master-slave D flip-flop configured as a divide-by-two. This architecture has the advantage of suppressing even-order harmonics of the frequency-doubled local oscillator (LO) signal and is insensitive to mismatches of the flip-flops.

The simplified circuit schematic shown in Figure 3 consists of 5 functional units of the modulator block diagram that have been merged: the two I/Q DACs, the two I/Q mixers, and the summer. The upper transistor level of the two current-mode logic trees is fully switched by the in-phase and quadrature LO. The second transistor level allows the generation of the 4 basic phase vectors of 0°, 180°, 90°, and 270°.

Figure 4 shows the quadrant that contains the first five phase states. The remaining three quadrants can be obtained by the inversion of the I and Q vectors. The ideal relative weights for the vector components are: 1, 0.924, 0.707, 0.383, and 0. An error of 1% in generating these values results in a phase error of up to 0.6°. The performance degradation due to α loss, and the mismatch of resistors and V_{be} can be minimized if the relative vector weights can be generated by the sum of integers. Integer values can easily be realized by identical current sources that match over process variations. The integer values 13, 12, 9, and 5 approximate the required relative weights. This approximation introduces a systematic phase error of up to 0.12° and an amplitude modulation of 0.18dB.

Further sources for phase errors are: 1) distortion, 2) LO leakage, 3) LO phase noise, 4) non-ideal I/Q generation of the LO, and 5) bias current dependent switching speed in the upper transistor level in Figure 3. 1) The total harmonic distortion of the DCA and the output buffer is lower than 0.8% and contributes to the total phase error by less than 0.2°. 2) A LO leakage of -30dB would result in an phase error of 2°. However LO leakage generated by the collector base capacitance is neutralized in the first-order by the inverted LO signal leakage (see upper transistor level in Figure 3). 3) Phase noise is determined largely by the loaded Q of the external tank circuit for the VCO.4) A phase error in the I/Q base vectors translates directly to an output phase error. Careful design of the DLL resulted in a maximum deviation of about 0.2° from the ideal 90° phase difference of the I and Q vectors. The remaining phase error is mainly a result of the bias-dependent switching speed in the upper transistor level. To reduce the simulated maximum absolute phase error of up to 3°, three additional current sources for error correction have been introduced in each DAC of the I and Q mixers (Figure 4). With this method the maximum absolute phase error could be reduced to 1.3° over process, voltage, and temperature variations. (The simulations do not include phase noise).

Table 1 summarizes measured data and the chip characteristics. Figure 5 shows the measured output spectrum. The three-IF-chip set (16-PSK modulator, receiver and 5b ADC) is fabricated in a two-metal level, 13GHz f_T (at V_{CE}=3V), silicon bipolar process. All chips were functional at first silicon. An implementation of the 16-PSK modulator in a 22GHz f_T (at V_{CE}=1V) production process and a power optimization could decrease the power consumption by a factor of 2. The die micrograph is shown in Figure 6. Three separated bias circuits are used to avoid interactions between the digital decoder, the PLL/DLL and the rest of the circuit.

Acknowledgments

The authors thank B. Hillery for transistor modelling and K. Kikuta for most of the layout.

References

[1] Bokulic, R. S., "Design of differential QPSK modulator", Electronics Letters, vol. 27, no. 13, pp. 1185-6, 1991.

[2] Feher, K., "Digital Communications", Prentice-Hall, 1981.

0-7803-0987-1 / 93 / $3.00 / ©1993 IEEE

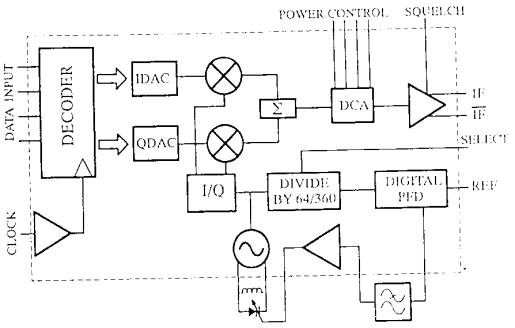

Figure 1: Block diagram of 16-PSK modulator chip.

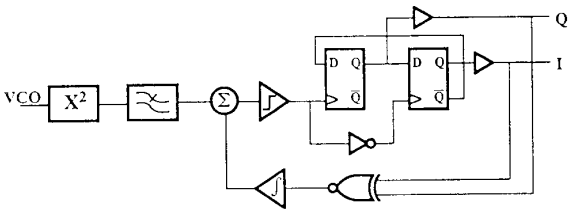

Figure 2: Simplified DLL block diagram.

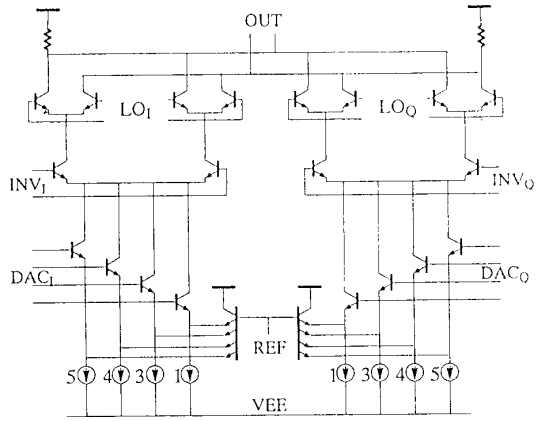

Figure 3: Schematic of I/Q DACs, mixer and summer.

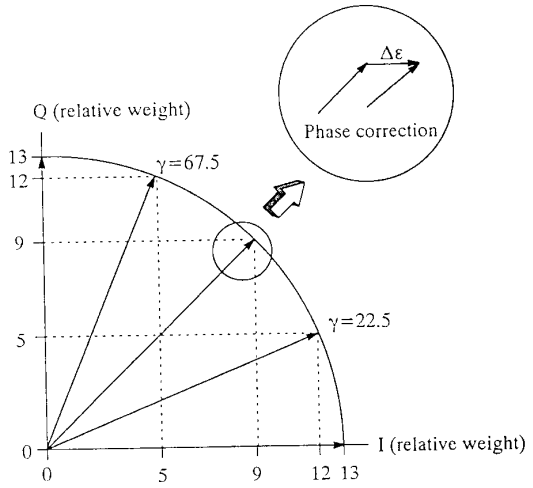

Figure 4: Phase generation by superposition of I and Q components of the LO.

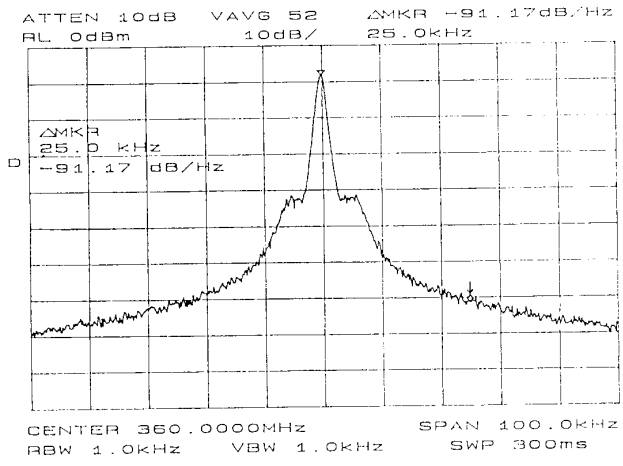

Figure 5: Measured output spectrum of the unmodulated IF.

Figure 6: See page 277.

Modulation schemes	2, 4, 8, 16-PSK
Maximum phase error	abs. 1.4°, rms: 0.2°
(16-PSK, 360MHz, dc data input)	
Maximum symbol rate	110Mb/s
IF range	200-400MHz
DCA range	70dB @ 360MHz
DCA step size	5dB
Maximum output power	+4dBm
Squelch attenuation	>100dB
Squelch switching time	<20ns
Single-sideband phase noise of LO (25kHz, external Q=40)	-90dBc
Power supplies	±5V
Power consumption	835mW
Temperature range	0°C-70°C
Chip size	4.3x4.5mm²
Package (with heat spreader)	68PLCC

Table 1: Chip performance and characteristics.

(Continued from page 135)

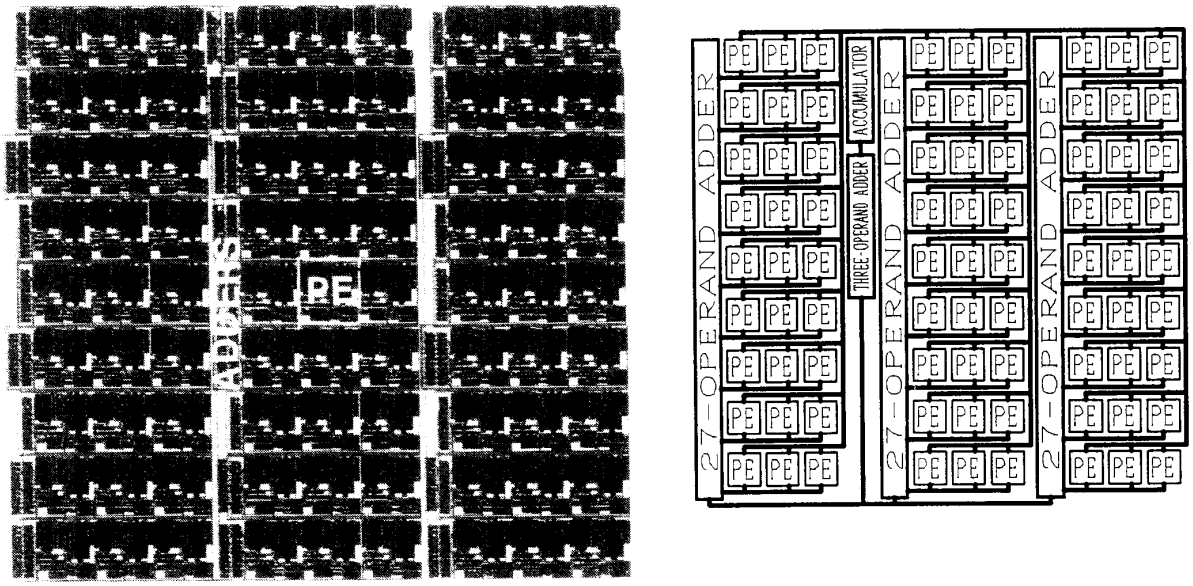

Figure 6: Residue-arithmetic VLSI processor.

TP 9.1: A 16-PSK Modulator with Phase Error Correction

(Continued from page 139)

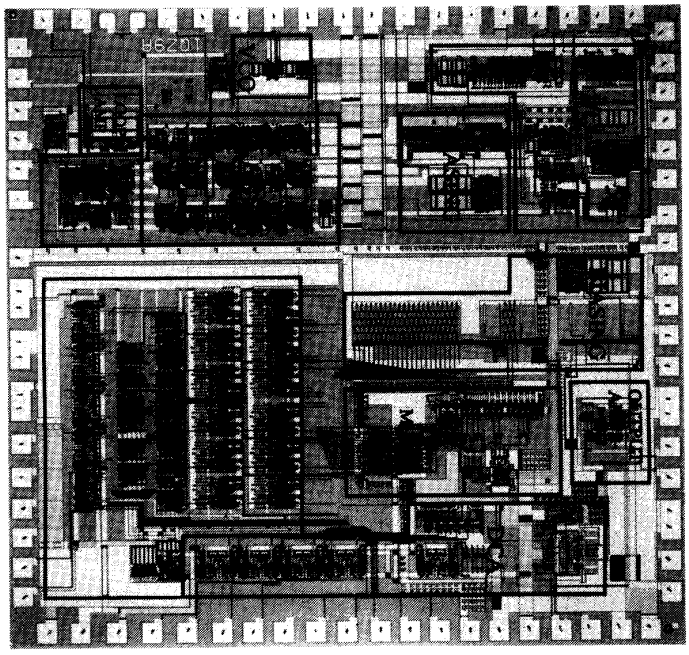

Figure 6: Micrograph of the 16-PSK modulator.