# Gigahertz CMOS/SIMOX Circuits

J.P. Colinge*, J. Kang, W. McFarland, C. Stout, R. Walker
Hewlett-Packard Laboratories, Palo Alto, CA
* Hewlett-Packard CT R&D, Palo Alto, CA
now with IMEC, Leuven, Belgium

High-speed CMOS logic circuits have been realized in thin-film (100 nm) SIMOX films annealed at 1250C. LOCOS isolation was used, and the gate oxide thickness was 22 nm. Boron concentration was 1E17 and 5E16 cm^{-3} in n- and p-channel devices, respectively. Since no silicide was used, source and drain sheet resistances was about 200 Ω/square. Only one level of metal was used. Since no kink is observed in thin-films, regular "nshort" and "pshort" SPICE models were used to simulate circuit operation. Most parameters can be easily introduced into SPICE (capacitances, mobility ...), but linear dependence of Vt on back gate has to be approximated by the square-root dependence included in SPICE. This introduces little error, however, in the 0-3.3 V supply voltage range. Circuits were realized with a gate mask length of 0.65 μm, corresponding to an effective gate length of 0.5 μm.

Circuits with the following performances were obtained (@ Vdd=3.3 V): 2:1 multiplexer operating at 1.4 Gbit/s (50 mW), voltage-controlled oscillator with an output frequency of up to 1.8 GHz (75 mW) and output stages with 250 ps rise and fall times (output impedance = 25 Ω). The output voltage swing is ECL, and a power dissipation of 65 mW is observed at a 312 Mbit/s data rate. A 2:1 frequency divider operating with an input frequency of 2 GHz and dissipating 12 mW was also fabricated. Simulation indicates 3 GHz operation if silicide was used, and higher speed performance should be obtained if circuit was realized with 2 metal levels.
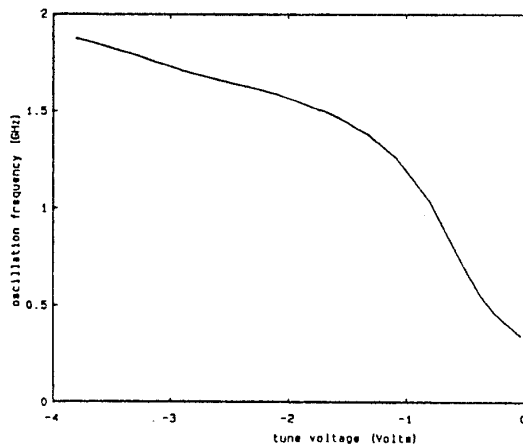
VCO tuning curve
Frequency (GHz) vs. input voltage
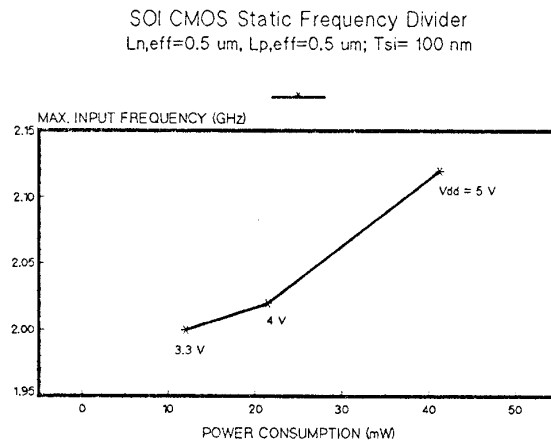
Frequency divider
Max. frequency vs. power consumption